



WatchDog function control for NCT5525D(Nuvoton)

By WadeLee

Step1: Type Index/data port into the configuration mode (2Eh/2Fh or 4Eh/4Fh)

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67 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
00 FF FF 00 FF FF FF FF 08 FF FF FF FF FF FF FF FF
10 DF DF FF 0C B8 FF FF FF FF FF 0B B3 1C 08 FF FF
20 D2 B3 F8 00 00 00 10 00 00 F0 00 00 07 FF 00 E4
30 01 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
40 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
50 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
60 0A 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF
70 FF FF FF FF FF FF FF FF 11111111 FF FF FF FF FF FF
80 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
90 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
A0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
B0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
C0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
D0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
E0 FF FF FF FF FF 00 00 00 FF 00 00 FF FF FF FF FF
F0 00 00 00 FF FF FF FF FF FF FF FF FF FF FF FF FF

Type: Indexed IO Port 002E,002F LDN 00
TAB Shift+TAB Next/Prev group of registers
    
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Step2: Set Rx07 as 08h to Select LDN device as watchdog timer

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67 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
00 FF FF 00 FF FF FF FF 08 FF FF FF FF FF FF FF FF
10 DF DF FF 0C B8 FF FF FF FF FF 0B B3 1C 08 FF FF
20 D2 B3 F8 00 00 00 10 00 00 F0 00 00 07 FF 00 E4
30 01 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
40 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
50 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
60 0A 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF
70 FF FF FF FF FF FF FF FF 11111111 FF FF FF FF FF FF
80 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
90 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
A0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
B0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
C0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
D0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
E0 FF FF FF FF FF 00 00 00 FF 00 00 FF FF FF FF FF
F0 00 00 00 FF FF FF FF FF FF FF FF FF FF FF FF FF

Type: Indexed IO Port 002E,002F LDN 00
TAB Shift+TAB Next/Prev group of registers
    
```

Step3: Set Rx30[0]=1 to active watchdog function

**21.6 Logical Device 8 (GPIO, WDT1)
CR 30h.**

Location: Address 30h
 Attribute: Read/Write
 Power Well: VCC
 Reset by: LRESET#
 Default : 01h
 Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	0: GPIO Base Address mode is inactive 1: GPIO Base Address mode is active
0	R / W	0: WDT1 is inactive. 1: WDT1 is active.

Step4: Set RxF0[3] to select count mode unit (Second / Minute mode)

CR F0h. Watchdog Timer I(WDT1) and KBC P20 Control Mode Register

Location: Address F0h
 Attribute: Read/Write
 Power Well: VCC
 Reset by: LRESET# or PWROK
 Default : 00h
 Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R / W	Select Watchdog Timer I count mode. 0: Second Mode. 1: Minute Mode.
2	R / W	Enable the rising edge of a KBC reset (P20) to issue a time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the Watchdog Timer I output low pulse to the KBRST# pin (Pin2) 0: Disable. 1: Enable.
0	R / W	Watchdog Timer I Pulse or Level mode select 0: Pulse mode 1: Level mode

Step5: Set RxF1 value to counter Timer (01h~FFh will auto count, set 00h has no action).
 The system will auto reset after this timer count down to 0.

CR F1h. Watchdog Timer I(WDT1) Counter Register

Location: Address F1h

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET# or PWROK

Default : 00h

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watch Dog Timer I Time-out value. Writing a non-zero value to the register causes the counter to load the value into the Watch Dog Counter and start counting down. The accuracy of watchdog timer I about one cycle deviation. If CR F2h, bits 7 and 6 are set, any Interrupt event comes from Mouse or Keyboard both cause the previously-loaded. Non-zero value will be reloaded to the Watch Dog Counter and the countdown resumes. Reading the register returns the current value in the Watch Dog Counter but not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after one cycle time, the cycle time is based on LD8 CRF0, bit[3], by analogy.