NEXCOM International Co., Ltd.

Network and Communication Solutions

Network Security Appliance

NSA 7160

User Manual

NEXCOM International Co., Ltd.
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PREFACE

Copyright

Disclaimer

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Acknowledgements

NSA 7160 are trademarks of NEXCOM International Co., Ltd. All other product names mentioned herein are registered trademarks of their respective owners.

Regulatory Compliance Statements

This section provides the FCC compliance statement for Class A devices and describes how to keep the system CE compliant.

Declaration of Conformity

FCC

This equipment has been tested and verified to comply with the limits for a Class A digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area (domestic environment) is likely to cause harmful interference, in which case the user will be required to correct the interference (take adequate measures) at their own expense.

CE

The product(s) described in this manual complies with all applicable European Union (CE) directives if it has a CE marking. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cable and cabling techniques.

RoHS Compliance

NEXCOM RoHS Environmental Policy and Status Update

NEXCOM is a global citizen for building the digital infrastructure. We are committed to providing green products and services, which are compliant with European Union RoHS (Restriction on Use of Hazardous Substance in Electronic Equipment) directive 2011/65/EU, to be your trusted green partner and to protect our environment.

RoHS restricts the use of Lead (Pb) < 0.1% or 1,000ppm, Mercury (Hg) < 0.1% or 1,000ppm, Cadmium (Cd) < 0.01% or 100ppm, Hexavalent Chromium (Cr6+) < 0.1% or 1,000ppm, Polybrominated biphenyls (PBB) < 0.1% or 1,000ppm, and Polybrominated diphenyl Ethers (PBDE) < 0.1% or 1,000ppm.

In order to meet the RoHS compliant directives, NEXCOM has established an engineering and manufacturing task force in to implement the introduction of green products. The task force will ensure that we follow the standard NEXCOM development procedure and that all the new RoHS components and new manufacturing processes maintain the highest industry quality levels for which NEXCOM are renowned.

The model selection criteria will be based on market demand. Vendors and suppliers will ensure that all designed components will be RoHS compliant.

How to recognize NEXCOM RoHS Products?

For existing products where there are non-RoHS and RoHS versions, the suffix "(LF)" will be added to the compliant product name.

All new product models launched after January 2013 will be RoHS compliant. They will use the usual NEXCOM naming convention.

Warranty and RMA

NEXCOM Warranty Period

NEXCOM manufactures products that are new or equivalent to new in accordance with industry standard. NEXCOM warrants that products will be free from defect in material and workmanship for 2 years, beginning on the date of invoice by NEXCOM.

NEXCOM Return Merchandise Authorization (RMA)

- Customers shall enclose the "NEXCOM RMA Service Form" with the returned packages.
- Customers must collect all the information about the problems encountered and note anything abnormal or, print out any on-screen messages, and describe the problems on the "NEXCOM RMA Service Form" for the RMA number apply process.
- Customers can send back the faulty products with or without accessories (manuals, cable, etc.) and any components from the card, such as CPU and RAM. If the components were suspected as part of the problems, please note clearly which components are included. Otherwise, NEXCOM is not responsible for the devices/parts.
- Customers are responsible for the safe packaging of defective products, making sure it is durable enough to be resistant against further damage and deterioration during transportation. In case of damages occurred during transportation, the repair is treated as "Out of Warranty."
- Any products returned by NEXCOM to other locations besides the customers' site will bear an extra charge and will be billed to the customer.

Repair Service Charges for Out-of-Warranty Products

NEXCOM will charge for out-of-warranty products in two categories, one is basic diagnostic fee and another is component (product) fee.

System Level

- Component fee: NEXCOM will only charge for main components such as SMD chip, BGA chip, etc. Passive components will be repaired for free, ex: resistor, capacitor.
- Items will be replaced with NEXCOM products if the original one cannot be repaired. Ex: motherboard, power supply, etc.
- Replace with 3rd party products if needed.
- If RMA goods can not be repaired, NEXCOM will return it to the customer without any charge.

Board Level

- Component fee: NEXCOM will only charge for main components, such as SMD chip, BGA chip, etc. Passive components will be repaired for free, ex: resistors, capacitors.
- If RMA goods can not be repaired, NEXCOM will return it to the customer without any charge.

Warnings

Read and adhere to all warnings, cautions, and notices in this guide and the documentation supplied with the chassis, power supply, and accessory modules. If the instructions for the chassis and power supply are inconsistent with these instructions or the instructions for accessory modules, contact the supplier to find out how you can ensure that your computer meets safety and regulatory requirements.

Cautions

Electrostatic discharge (ESD) can damage system components. Do the described procedures only at an ESD workstation. If no such station is available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the computer chassis.

Safety Information

Before installing and using the device, note the following precautions:

- Read all instructions carefully.
- Do not place the unit on an unstable surface, cart, or stand.
- Follow all warnings and cautions in this manual.
- When replacing parts, ensure that your service technician uses parts specified by the manufacturer.
- Avoid using the system near water, in direct sunlight, or near a heating device.
- The load of the system unit does not solely rely for support from the rackmounts located on the sides. Firm support from the bottom is highly necessary in order to provide balance stability.
- The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Installation Recommendations

Ensure you have a stable, clean working environment. Dust and dirt can get into components and cause a malfunction. Use containers to keep small components separated.

Adequate lighting and proper tools can prevent you from accidentally damaging the internal components. Most of the procedures that follow require only a few simple tools, including the following:

- A Philips screwdriver
- A flat-tipped screwdriver
- A grounding strap
- An anti-static pad

Using your fingers can disconnect most of the connections. It is recommended that you do not use needle-nose pliers to disconnect connections as these can damage the soft metal or plastic parts of the connectors.

Safety Precautions

1. Read these safety instructions carefully.

2. Keep this User Manual for later reference.

3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.

4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.

5. Keep this equipment away from humidity.

6. Put this equipment on a stable surface during installation. Dropping it or letting it fall may cause damage.

7. The openings on the enclosure are for air convection to protect the equipment from overheating. DO NOT COVER THE OPENINGS.

8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.

9. Place the power cord in a way so that people will not step on it. Do not place anything on top of the power cord. Use a power cord that has been approved for use with the product and that it matches the voltage and current marked on the product's electrical range label. The voltage and current rating of the cord must be greater than the voltage and current rating marked on the product.

10. All cautions and warnings on the equipment should be noted.

11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.

12. Never pour any liquid into an opening. This may cause fire or electrical shock.

13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.

14. If one of the following situations arises, get the equipment checked by service personnel:
    a. The power cord or plug is damaged.
    b. Liquid has penetrated into the equipment.
    c. The equipment has been exposed to moisture.
    d. The equipment does not work well, or you cannot get it to work according to the user's manual.
    e. The equipment has been dropped and damaged.
    f. The equipment has obvious signs of breakage.

15. Do not place heavy objects on the equipment.

16. The unit uses a three-wire ground cable which is equipped with a third pin to ground the unit and prevent electric shock. Do not defeat the purpose of this pin. If your outlet does not support this kind of plug, contact your electrician to replace your obsolete outlet.

17. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER. DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

Technical Support and Assistance

1. For the most updated information of NEXCOM products, visit NEXCOM's website at www.nexcom.com.

2. For technical issues that require contacting our technical support team or sales representative, please have the following information ready before calling:
   - Product name and serial number
   - Detailed information of the peripheral devices
   - Detailed information of the installed software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wordings of the error messages

Warning!

1. Handling the unit: carry the unit with both hands and handle it with care.

2. Maintenance: to keep the unit clean, use only approved cleaning products or clean with a dry cloth.

Conventions Used in this Manual

Warning:
Information about certain situations, which if not observed, can cause personal injury. This will prevent injury to yourself when performing a task.

Caution:
Information to avoid damaging components or losing data.

Note:
Provides additional information to complete a task easily.

Global Service Contact Information

Headquarters

NEXCOM International Co., Ltd.

9F, No. 920, Zhongzheng Rd.,
Zhonghe District, New Taipei City, 23586,
Taiwan, R.O.C.
Tel: +886-2-8226-7786
Fax: +886-2-8226-7782
www.nexcom.com

Asia

Taiwan

NexAIoT Headquarters
Industry 4.0 and Cloud Services

13F, No.922, Zhongzheng Rd.,
Zhonghe District, New Taipei City,
23586, Taiwan, R.O.C.
Tel: +886-2-8226-7796
Fax: +886-2-8226-7926
Email: jacobhuang@nexaiot.com
www.nexaiot.com

NexAIoT Co., Ltd.
Taichung Office

16F, No.250, Sec.2, Chongde Rd.,
Beitun District,
Taichung City, 406, Taiwan, R.O.C.
Tel: +886-4-2249-1179
Fax: +886-4-2249-1172
Email: jacobhuang@nexaiot.com
www.nexaiot.com

NexCOBOT Taiwan Co., Ltd.

13F, No.916, Zhongzheng Rd.,
Zhonghe District,
New Taipei City, 23586, Taiwan, R.O.C.
Tel: +886-2-8226-7786
Fax: +886-2-8226-7926
Email: jennyshern@nexcobot.com
www.nexcobot.com

GreenBase Technology Corp.

13F, No.922, Zhongzheng Rd.,
Zhonghe District,
New Taipei City, 23586, Taiwan, R.O.C.
Tel: +886-2-8226-7786
Fax: +886-2-8226-7900
Email: vivianlin@nexcom.com.tw
www.nexcom.com.tw

DivioTec Inc.

19F-1A, No.97, Sec.4, ChongXin Rd.,
Sanchong District,
New Taipei City, 24161, Taiwan, R.O.C.
Tel: +886-2-8976-3077
Email: sales@diviotec.com
www.diviotec.com

AIoT Cloud Corp.

13F, No.922, Zhongzheng Rd.,
Zhonghe District,
New Taipei City, 23586, Taiwan, R.O.C.
Tel: +886-2-8226-7786
Fax: +886-2-8226-7782
Email: alantsai@aiotcloud.net
www.aiotcloud.dev

EMBUX TECHNOLOGY CO., LTD.

13F, No.916, Zhongzheng Rd.,
Zhonghe District,
New Taipei City, 23586, Taiwan, R.O.C.
Tel: +886-2-8226-7786
Fax: +886-2-8226-7782
Email: info@embux.com
www.embux.com

TMR TECHNOLOGIES CO., LTD.

13F, No.916, Zhongzheng Rd.,
Zhonghe District,
New Taipei City, 23586, Taiwan, R.O.C.
Tel: +886-2-8226-7786
Fax: +886-2-8226-7782
Email: services@tmrtek.com
www.tmrtek.com

China

NEXSEC Incorporated

201, Floor 2, Unit 2, Building 15, Yard 3,
Gaolizhang Road, Haidian District,
Beijing, 100094, China
Tel: +86-10-5704-2680
Fax: +86-10-5704-2681
Email: marketing@nexsec.cn
www.nexsec.cn

NEXCOM Shanghai

Room 406-407, Building C, No 154, Lane 953,
Jianchuan Road, Minhang District,
Shanghai, 201108, China
Tel: +86-21-5278-5868
Fax: +86-21-3251-6358
Email: sales@nexcom.cn
www.nexcom.cn

NEXCOM Surveillance Technology Corp.

Floor 8, Building B3, Xiufeng Industrial Zone,
GanKeng Community, Buji Street,
LongGang District,
ShenZhen, 518112, China
Tel: +86-755-8364-7768
Fax: +86-755-8364-7738
Email: steveyang@nexcom.com.tw
www.nexcom.cn

NEXGOL Chongqing

1st Building No.999,
Star Boulevard, Yongchuan Dist,
Chongqing City, 402160, China
Tel: +86-23-4960-9080
Fax: +86-23-4966-5855
Email: sales@nexgol.com.cn
www.nexcom.cn

Beijing NexGemo Technology Co.,Ltd.

Room 205, No.1, Fazhan Rd.,
Beijing International Information Industry Base,
Changping District,
Beijing, 102206, China
Tel: +86-10-8072-2025
Fax: +86-10-8072-2022
Email: sales@nexgemo.cn
www.nexgemo.com

Japan

NEXCOM Japan

9F, Tamachi Hara Bldg.,
4-11-5, Shiba Minato-ku,
Tokyo, 108-0014, Japan
Tel: +81-3-5419-7830
Fax: +81-3-5419-7832
Email: sales@nexcom-jp.com
www.nexcom-jp.com

America

USA

NEXCOM USA

46665 Fremont Blvd.,
Fremont CA 94538, USA
Tel: +1-510-656-2248
Fax: +1-510-656-2158
Email: sales@nexcom.com
www.nexcomusa.com

Package Contents

Before continuing, verify that the NSA 7160 package that you received is complete. Your package should have all the items listed in the following table.

Item	Part Number	Name	Qty
1	19S00716000X0	NSA7160 ASSY	1
2	5050301098X00	(N)CPU HEATSINK FOR NSA7160 VER:A DELTA	2
3	50311F0110X00	(H)FLAT HEAD SCREW LONG FEI:F3x5ISO+NYLOK NIGP	8
4	5044440031X00	RUBBER FOOT KANG YANG:RF20-5-4P	4
5	6012200052X00	PE ZIPPER BAG #8 炎洲:印刷由任袋8號	1
6	6012200053X00	PE ZIPPER BAG #3 炎洲:印刷由任袋3號	1
7	6023309081X00	CABLE EDI:232091081804-RS	1
8	60110A0301X00	ACCESSORY BOX FOR NSA7150 SERIES HEATSINK VER:A YI GIA	1
9	50311F0162X00	(H)ROUND HEAD SCREW GW/WASHER LONG FEI	1
10	60110A0229X00	ACCESSORY BOX FOR S2216/S2224 VER:A YI GIA	2
11	5040290005X00	EAR SET FOR NSA7145 (BRAND:4ipnet) VER:A PANADVANCE	1
12	5040150001X00	NSA7135 AL HANDLE VER:A PANADVANCE	1
13	6012200096X00	PE BAG FOR UTM625 VAR:A CHYUAN-JYH	1
14	50311F0713X00	I HEAD T8 SCREW LONG FEI	1
15	4NCIF00202X00	MINI JUMPER 1x2 CATCH:1133-001-02	1
16	5061600324H00	(N)LGA4677 CPU SOCKET CARRIER FOXCONN:WNMEC00-0NNK2-EH	2
17	5061600310H00	(N)LGA4677 CPU SOCKET CARRIER FOXCONN:WNMEC00-0NNK1-EH	2
18	6014607063X00	LABEL FOR NSA7160 HEATSINK VER:A KIN-SHINE	2
19	60111A0980X00	(N)INNER CARTON FOR NSA7160 VER:A YI GIA	1
20	60111A0981X00	(N)OUTSIDE CARTON FOR NSA7160 VER:A YI GIA	1
21	6013301858X00	(N)EPE REAR BOTTOM FOR NSA7160 VER:A TSAIJIN	1
22	6013301859X00	(N)EPE FRONT BOTTOM FOR NSA7160 VER:A TSAIJIN	1
23	6013301860X00	(N)EPE REAR TOP FOR NSA7160 VER:A TSAIJIN	1
24	6013301861X00	(N)EPE FRONT TOP FOR NSA7160 VER:A TSAIJIN	1
25	6013301862X00	(N)EPE FOR NSA7160 HEATSINK VER:A TSAIJIN	4

Ordering Information

The following information below provides ordering information for NSA 7160.

Barebone

NSA 7160 (P/N: 10S00716000X0)

2U w/ Dual 4th Gen Intel® Xeon® Scalable processor w/ QAT, LCM,
8 x LAN module slots

Supported LAN Modules

LAN Module	P/N	Interface	Type	Port Number	Bypass/ Segment	Expansion Slot	Speed	Location Slot
NI 140C-OS	2BS10140C00X0	i350AM4x1	PCIex4	4xRJ45	0	None	1G	All
NI 142CX1-OS	2BS10142C00X0	i350AM4x1	PCIex4	4xRJ45	2	None	1G	All
NI 180C-OS	2BS10180C00X0	i350AM4x2	2xPCIex4	8xRJ45	0	None	1G	All
NI 184CX1-OS	2BS10184C02X0	i350AM4x2	2xPCIex4	8xRJ45	4	None	1G	All
NI 180F-OS	2BS10180C17X0	i350AM4 x 2	2xPCIex4	8xSFP+	0	None	1G	All
NX 120F-OS	2BS20120F00X0	X710-BM2	PCIx8	2xSFP+	0	None	10G	All
NX 140F-OS	2BS20140F02X0	XL710-BM1	PCIx8	4xSFP+	0	None	10G	All
NX 142FX1-OS	2BS20142F01X0	XL710-BM1	PCIx8	4 SFP+ LC	2	None	10G	All
NX 142FX1-LR-OS	2BS20142F02X0	XL710-BM1	PCIx8	4 SFP+ LC	2	None	10G	All
NX 121FX1-OS	2BS20121F02X0	X710-BM2	PCIx8	2 SFP+ LC	1	None	10G	All
NX 121FX1-LR-OS	2BS20121F03X0	X710-BM2	PCIx8	2 SFP+ LC	1	None	10G	All
NC 120FIS4-OS	2BS30012001X0	E810-CAM2	PCIex16 (Gen 4)	2 xQSFP28	0	None	100G	All
NL 110FM-OS	2BS60011000X0	MT28924A0-NCCF-VE	PCIex16 (Gen 4)	1 x QSFP28/56	0	None	200G	All

Module slot order and positions

Basically, all the supported LAN modules mentioned above can be plugged into any of the slots. However, it is recommended to follow the order indicated in the right image when plugging in the LAN modules.

Chapter 1: Product Introduction

Overview

Key Features

- Dual 4th Gen Intel® Xeon® scalable processor
- 16 x DDR5 4800 ECC RDIMM
- 2 x 2.5” swappable SSD/HDD
- 2 x Management ports
- 1300W 1+1 CRPS redundant power supply
- 8 x PCIe 5 LAN module slots
- 1 x PCIe 4 x16 slot for FHFL card
- Supports 1 x IPMI 2.0 RunBMC (optional)

Hardware Specifications

Main Board

- Dual Intel® 4th Gen Xeon® Scalable processor, socket LGA 4677
- PCH: Intel® Emmitsburg (C741)
- Supports 4 x UPI between CPUs
- TPM 2.0 onboard

Memory

- 16 (8+8) DDR5 memory DIMMs, up to 1024GB per RDIMM

Storage

- 2 x 2.5" swappable SSD/HDD
- 1 x M.2 2280 (Key M) socket

Interface-External

- Button: Power & reset & NMI
- LED: PWR/STBY/HDD/ERR
- 2 x 2.5" swappable SSD/HDD bays
- 2 x USB 3.0 ports
- 1 x RJ45 type console
- 8 x PCIe5 LAN module slots
- 2 x Management ports (1 x RJ45 & 1 x SFP)
- 1 x VGA port (for models with BMC installed only)
- 3 x Swappable smart fans
- 2 x Power inlets
- 1 x LCM module

Interface-Internal

- 1 x RunBMC module connector
- 1 x PCIe 4 x16 slot with CXL1.1 for FHFL card

Power Input

- 1300W 1+1 CRPS redundant power supply

Dimensions and Weight

- Chassis dimension: 438 mm x 800 mm x 88 mm
- Carton dimension: 1015 x 688 x 285 mm
- Without packing: 21.9 Kg
- With packing: 35.87 Kg

Environment

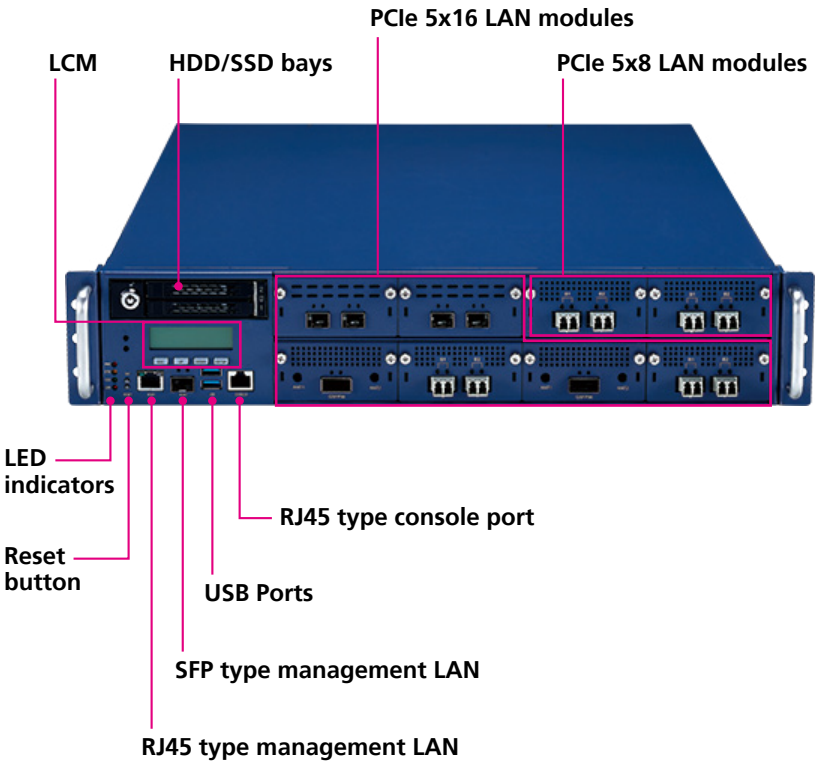
- Operating temperature: 0°C~40°C
- Storage temperature: -20°C~75°C
- Relative humidity: 10%~90% non-condensing

Certifications

- CE/FCC Class A
- UL

Knowing Your NSA 7160

Front Panel



LCM (Liquid Crystal Display Module)
Reserved for the user to define.

HDD/SDD Bays
Two 2.5" HDD/SSD swappable bays for installing HDD/SSDs.

LED Indicators
Indicates the power status, error status, and storage drive activity of the system.

Reset Button
Press to restart the system.

RJ45 Type Management LAN Port
RJ45 type LAN port used for managing the system.

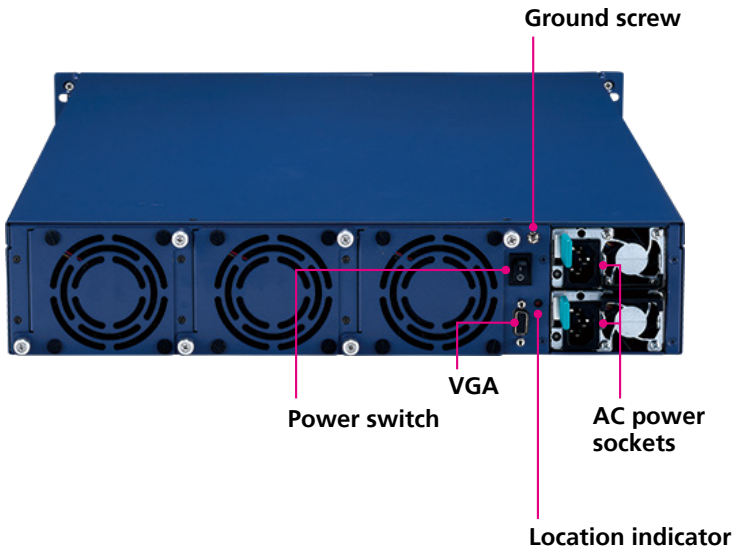
SFP Type Management LAN Port
SFP port used for managing the system.

USB Ports
Used to connect USB 3.0/2.0/1.1 devices.

RJ45 Type Console Serial Port
Used to connect console device with RJ45 type connection.

LAN Modules
PCIe 5x16 LAN modules. (SFF OCP 4C+ standard interface)
PCIe 5x8 LAN modules. (SFF OCP 4C+ standard interface)

Rear Panel



Power Switch
Press to power-on or power-off the system.

VGA
Used to connect an analog VGA monitor.

Location Indicator
Used to indicate the location of the unit using the remote control.

AC Power Sockets
Dual redundant power supply sockets, plug an AC power cord here before turning on the system.

Ground Screw
The round head screw included in the accessory pack (P/N: 50311F0162X00) can be installed here as the ground screw. Ensure that the ground screw is installed first before use.

Chapter 2: Jumpers and Connectors

This chapter describes how to set the jumpers and connectors on the NSA 7160 motherboard.

Before You Begin

- Ensure you have a stable, clean working environment. Dust and dirt can get into components and cause a malfunction. Use containers to keep small components separated.
- Adequate lighting and proper tools can prevent you from accidentally damaging the internal components. Most of the procedures that follow require only a few simple tools, including the following:
  - A Philips screwdriver
  - A flat-tipped screwdriver
  - A set of jewelers screwdrivers
  - A grounding strap
  - An anti-static pad
- Using your fingers can disconnect most of the connections. It is recommended that you do not use needle-nosed pliers to disconnect connections as these can damage the soft metal or plastic parts of the connectors.
- Before working on internal components, make sure that the power is off. Ground yourself before touching any internal components, by touching a metal object. Static electricity can damage many of the electronic components. Humid environments tend to have less static electricity than dry environments. A grounding strap is warranted whenever danger of static electricity exists.

Precautions

Computer components and electronic circuit boards can be damaged by discharges of static electricity. Working on computers that are still connected to a power supply can be extremely dangerous.

Follow the guidelines below to avoid damage to your computer or yourself:

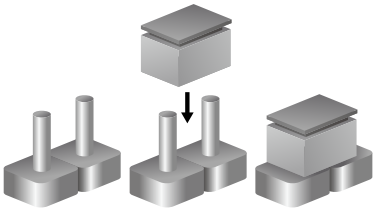
- Always disconnect the unit from the power outlet whenever you are working inside the case.
- If possible, wear a grounded wrist strap when you are working inside the computer case. Alternatively, discharge any static electricity by touching the bare metal chassis of the unit case, or the bare metal body of any other grounded appliance.
- Hold electronic circuit boards by the edges only. Do not touch the components on the board unless it is necessary to do so. Don't flex or stress the circuit board.
- Leave all components inside the static-proof packaging that they shipped with until they are ready for installation.
- Use correct screws and do not over tighten screws.

Jumper Settings

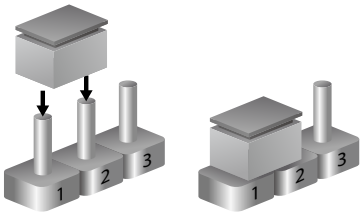
A jumper is the simplest kind of electric switch. It consists of two metal pins and a cap. When setting the jumpers, ensure that the jumper caps are placed on the correct pins. When the jumper cap is placed on both pins, the jumper is short. If you remove the jumper cap, or place the jumper cap on just one pin, the jumper is open.

Refer to the illustrations below for examples of what the 2-pin and 3-pin jumpers look like when they are short (on) and open (off).

Two-Pin Jumpers: Open (Left) and Short (Right)

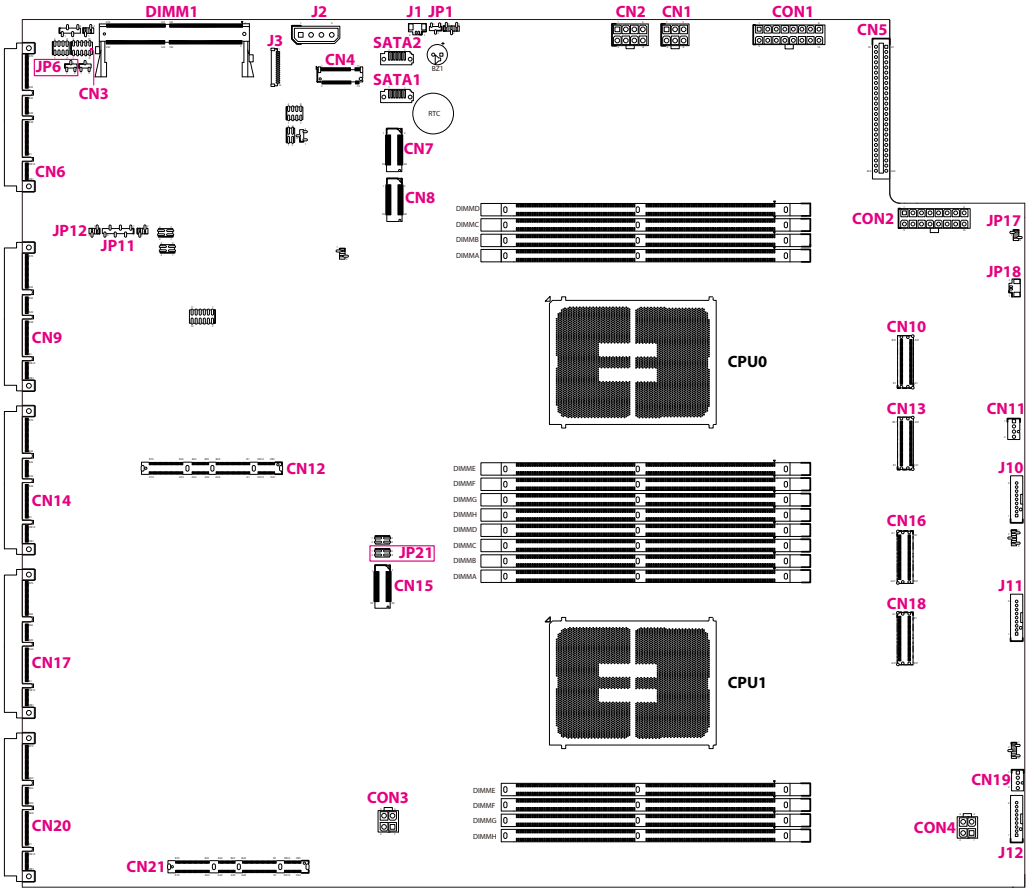


Three-Pin Jumpers: Pins 1 and 2 are Short



Locations of the Jumpers and Connectors

The right figure shows the location of the jumpers and connectors. For more detailed information on pin settings and definitions marked in pink on this figure, please refer to this chapter.



It is strongly not recommended to adjust the jumpers that are not mentioned in this chapter.

Jumper

RTC Clear

Connector type: 1X3 3-Pin
Connector location: JP1

Pin	Definition
1	NC
2	RST_RTCRST_N
3	GND

Pin	Settings
1-2 On	Normal (Default)
2-3 On	Clear CMOS

AT/ATX Header

Connector type: 1x3 3-pin header
Connector location: JP6

Pin	Definition
1	P3V3_CPLD
2	AT_ATX_SEL
3	GND

Pin	Settings
1-2 On	ATX (Default)
2-3 On	AT

CPLD JTAG Select

Connector type: 2X1 2-Pin
Connector location: JP12

Pin	Definition
1	JTAG_SEL
2	GND

Pin	Settings
NC	BMC to CPLD JTAG pin (Default)
1-2 On	JTAG header to CPLD JTAG pin

Boot Guard Debug Strap Header

Connector type: 2X2 4-Pin
Connector location: JP21

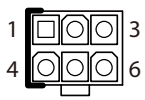
Pin	Definition
1	GND
2	PD_CPU0_TXT_PLTEN
3	GND
4	PD_CPU1_TXT_PLTEN

Pin	Settings
1-2 On 3-4 On	Disable boot guard (Default)
1-2 Off 3-4 Off	Enable boot guard

Internal Connectors

Power Connector (CN1 to Riser Board)

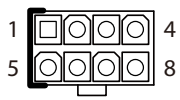
Connector type: 2X3 6-Pin
Connector location: CN1



Pin	Definition
1	GND
2	GND
3	GND
4	P12V
5	P12V
6	P12V

Power Connector (CN2 to FHFL Card)

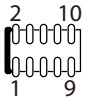
Connector type: 2X4 8-Pin
Connector location: CN2



Pin	Definition
1	GND
2	GND
3	GND
4	GND
5	P12V
6	P12V
7	P12V
8	P12V

GPIO Header

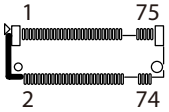
Connector type: 2x5 10-pin header
Connector location: CN3



Pin	Definition	Pin	Definition
1	P3V3_CPLD	6	CPLD_GPO02
2	GND	7	CPLD_GPI03
3	CPLD_GPI01	8	CPLD_GPO03
4	CPLD_GPO01	9	CPLD_GPI04
5	CPLD_GPI02	10	CPLD_GPO04

M.2 Key M Connector

Connector type: 2280 75-pin header
Connector location: CN4

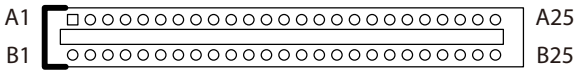


Pin	Definition	Pin	Definition
1	NGFF_CONFIG_3	18	P3V3
2	P3V3	19	PCIE_RX_M2_R_2_DP
3	GND	20	NC
4	P3V3	21	NGFF_CONFIG_0
5	PCIE_RX_M2_R_3_DN	22	NC
6	NC	23	PCIE_TX_M2_R_2_DN
7	PCIE_RX_M2_R_3_DP	24	NC
8	NC	25	PCIE_TX_M2_R_2_DP
9	GND	26	NC
10	NGFF_DSSN	27	GND
11	PCIE_TX_M2_R_3_DN	28	NC
12	P3V3	29	PCIE_RX_M2_R_1_DN
13	PCIE_TX_M2_R_3_DP	30	NC
14	P3V3	31	PCIE_RX_M2_R_1_DP
15	GND	32	NC
16	P3V3	33	GND
17	PCIE_RX_M2_R_2_DN	34	NC

Pin	Definition	Pin	Definition
35	PCIE_TX_M2_R_1_DN	52	FM_CLKREQ_M2_1_N
36	NC	53	CLK_100M_M2_DN
37	PCIE_TX_M2_R_1_DP	54	IRQ_LVC3_WAKE_N
38	NGFF_DEVSLP	55	CLK_100M_M2_DP
39	GND	56	NC
40	N30398252	57	GND
41	PCIE_RX_M2_R_0_DP	58	NC
42	N30398249	67	NC
43	PCIE_RX_M2_R_0_DN	68	PCH_SUSCLK_33K_R_SSD
44	NC	69	FM_M2_1_PEDET
45	GND	70	P3V3
46	NC	71	GND
47	PCIE_TX_M2_R_0_DN	72	P3V3
48	NC	73	GND
49	PCIE_TX_M2_R_0_DP	74	P3V3
50	PE_RST_M2_N	75	NGFF_CONFIG_2
51	GND		

Power Connector (To Power Board)

Connector type: 2X25 50-Pin
Connector location: CN5

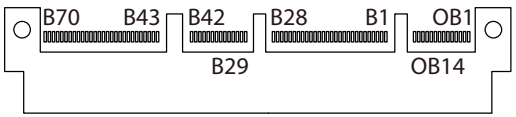


Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	P12V	B10	P12V
A11	P12V	B11	P12V
A12	P12V	B12	P12V
A13	P12V	B13	P12V

Pin	Definition	Pin	Definition
A14	P12V	B14	P12V
A15	P12V	B15	P12V
A16	P12V	B16	P12V
A17	P12V	B17	P12V
A18	P12V	B18	P12V
A19	SMB_PFR_PMB1_STBY_LVC3_CRPS_SDA	B19	GND
A20	SMB_PFR_PMB1_STBY_LVC3_CRPS_SCL	B20	FM_PS_EN_PSU_N
A21	GND	B21	P12V_STBY_PSU
A22	IRQ_SML1_PMBUS_BMC_ALERT_N	B22	RETURN_SENSE
A23	PWRGD_PS_PWROK	B23	CRPS_PRESEND1
A24	AC_FAIL_PSU	B24	12V_REMOTE_SENSE
A25	P3V3_CPLD	B25	CRPS_PRESEND2

IO Slot Connector (for NSK1107 only)

Connector type: 2x84 168-pin header
Connector location: CN6



Pin	Definition	Pin	Definition
OA1	P3V3_AUX	OB1	P12V
OA2	P3V3_AUX	OB2	P12V
OA3	P3V3_AUX	OB3	GND
OA4	GND	OB4	P3V3_CPLD
OA5	P3V3_BMC	OB5	P3V3_CPLD
OA6	P3V3_BMC	OB6	P3V3_CPLD
OA7	GND	OB7	GND
OA8	NVM_SO_A	OB8	P3V3
OA9	NVM_SI_A	OB9	P3V3
OA10	GND	OB10	GND

Pin	Definition	Pin	Definition
OA11	NVM_SK_B	OB11	NVM_SK_A
OA12	GND	OB12	GND
OA13	GND	OB13	GND
OA14	GND	OB14	GND
A1	GND	B1	P5V
A2	GND	B2	P5V
A3	GND	B3	P5V
A4	GND	B4	P5V
A5	GND	B5	P5V
A6	GND	B6	P5V
A7	NVM_CS_N_A	B7	GND
A8	NVM_CS_N_B	B8	GND
A9	NVM_SO_B	B9	GND
A10	GND	B10	GND
A11	NVM_SI_B	B11	GND

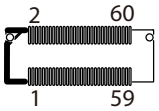
Note that the definition on this connector is not the standard pin definition of an OCP connector.

Pin	Definition	Pin	Definition
A12	GND	B12	GND
A13	GND	B13	GND
A14	USB3_P06_TXN	B14	USB3_P06_RXN
A15	USB3_P06_TXP	B15	USB3_P06_RXP
A16	GND	B16	GND
A17	USB3_P07_TXN	B17	USB3_P07_RXN
A18	USB3_P07_TXP	B18	USB3_P07_RXP
A19	GND	B19	GND
A20	USB2_P7_IO_DN	B20	USB2_P6_IO_DN
A21	USB2_P7_IO_DP	B21	USB2_P6_IO_DP
A22	GND	B22	GND
A23	CLK_100M_I210_LANA_DP	B23	CLK_100M_I210_LANB_DP
A24	CLK_100M_I210_LANA_DN	B24	CLK_100M_I210_LANB_DN
A25	GND	B25	GND
A26	PCIE_TX_LANB_DP	B26	PCIE_RX_LANB_DP
A27	PCIE_TX_LANB_DN	B27	PCIE_RX_LANB_DN
A28	GND	B28	GND
A29	GND	B29	GND
A30	PCIE_TX_LANA_DP	B30	PCIE_RX_LANA_DP
A31	PCIE_TX_LANA_DN	B31	PCIE_RX_LANA_DN
A32	GND	B32	GND
A33	SMB_LANA_CLK_R	B33	NCSI_TXD0_A
A34	SMB_LANA_DATA_R	B34	GND
A35	GND	B35	GND
A36	BMC_R_TXD5	B36	NCSI_TXD1_A
A37	BMC_R_RXD5	B37	GND
A38	GND	B38	GND
A39	CPLD_UART_TXD	B39	NCSI_CLK_I210_R1_A
A40	CPLD_UART_RXD	B40	GND
A41	GND	B41	GND

Pin	Definition	Pin	Definition
A42	GND	B42	NCSI_TX_EN_A
A43	GND	B43	GND
A44	SIO_LCM_TXD	B44	NCSI_RXD0_A
A45	SIO_LCM_RXD	B45	GND
A46	GND	B46	GND
A47	SIO_LCM_LED_KR	B47	NCSI_RXD1_A
A48	SIO_LCM_LED_KG	B48	GND
A49	GND	B49	GND
A50	LED_PCH_HDD_IOCARD	B50	NCSI_CRS_DV_A
A51	IO_ALERT_LED#	B51	GND
A52	GND	B52	GND
A53	POWER_ERROR_LED	B53	LED_PWR_STBY_ON
A54	GND	B54	GND
A55	GND	B55	GND
A56	GND	B56	NMI_BTN_N_L
A57	GND	B57	GND
A58	GND	B58	GND
A59	GND	B59	FM_OC3_USB_N
A60	GND	B60	GND
A61	GND	B61	GND
A62	GND	B62	FM_I210_WAKE_N
A63	GND	B63	GND
A64	GND	B64	GND
A65	GND	B65	PE_RST_LAN_N
A66	GND	B66	GND
A67	GND	B67	GND
A68	GND	B68	FP_RST_BTN_N_L
A69	GND	B69	GND
A70	GND	B70	GND

XDP Debug Connector (For PCH)

Connector type: 2x30 60-pin header
Connector location: CN7

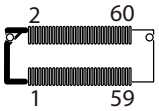


Pin	Definition	Pin	Definition
1	P1V05_PCH_AUX	16	GND
2	JTAG_DBP_TMS_R	17	FM_DBP_PRESENT_R_N
3	JTAG_DBP_CPU_TCK_R	18	NC
4	JTAG_DBP_TDO_R	19	TRC_PCH_PTI0
5	JTAG_DBP_TDI_R	20	NC
6	RST_DBP_RST_CO_N	21	TRC_PCH_PTI1
7	DBP_PMODE	22	NC
8	PD_TRST_PD3	23	TRC_PCH_PTI2
9	NC	24	NC
10	H_DBP_PREQ_N_R	25	TRC_PCH_PTI3
11	H_DBP_PRDY_R_N	26	NC
12	P1V8_PCH_AUX	27	TRC_PCH_PTI4
13	TRC_PCH_PTI0_CLK	28	NC
14	GND	29	TRC_PCH_PTI 5
15	DBP_PCH_DEBUG_ CONSENT_N	30	NC

Pin	Definition	Pin	Definition
31	TRC_PCH_PTI 6	46	NC
32	NC	47	TRC_PCH_PTI14
33	TRC_PCH_PTI 7	48	SMB_HOST_STBY_LVC3_ XDP_SCL
34	NC	49	TRC_PCH_PTI15
35	TRC_PCH_PTI 8	50	SMB_HOST_STBY_LVC3_ XDP_SDA
36	DBP_BOOT_HALT_N	51	JTAG_DBP_PCH_R_TCK
37	TRC_PCH_PTI 9	52	P3V3_AUX
38	FM_CPU_FBRK_DEBUG_N	53	DBP_CPU_HOOK9_MBP3_N
39	TRC_PCH_PTI10	54	NC
40	DBP_POWER_BTN_N	55	DBP_CPU_HOOK8_MBP2_N
41	TRC_PCH_PTI11	56	NC
42	RST_DBP_RSMRST_N	57	GND
43	TRC_PCH_PTI12	58	GND
44	NC	59	TRC_PCH_PTI1_CLK
45	TRC_PCH_PTI13	60	GND

XDP Debug Connector (For CPU1)

Connector type: 2x30 60-pin header
Connector location: CN8

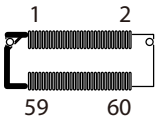


Pin	Definition	Pin	Definition
1	PD_CPU0_DBP_PIN1	16	GND
2	NC	17	GND
3	NC	18	TRC_CPU0_PTI10
4	NC	19	TRC_CPU0_PTI00
5	NC	20	TRC_CPU0_PTI11
6	NC	21	TRC_CPU0_PTI01
7	NC	22	TRC_CPU0_PTI12
8	PD_TRST_CPU0	23	TRC_CPU0_PTI02
9	NC	24	TRC_CPU0_PTI13
10	NC	25	TRC_CPU0_PTI03
11	NC	26	TRC_CPU0_PTI14
12	PVNN_TERM_CPU0	27	TRC_CPU0_PTI04
13	TRC_CPU0_PTI0_CLK0	28	TRC_CPU0_PTI15
14	TRC_CPU0_PTI1_CLK0	29	TRC_CPU0_PTI05
15	GND	30	TRC_CPU0_PTI16

Pin	Definition	Pin	Definition
31	TRC_CPU0_PTI06	46	TRC_CPU0_PTI111
32	TRC_CPU0_PTI17	47	TRC_CPU0_PTI014
33	TRC_CPU0_PTI07	48	TRC_CPU0_PTI112
34	NC	49	TRC_CPU0_PTI015
35	TRC_CPU0_PTI08	50	TRC_CPU0_PTI113
36	NC	51	NC
37	TRC_CPU0_PTI09	52	P3V3_AUX
38	TRC_CPU0_PTI18	53	DBP_CPU0_HOOK9_MBP3_QS_R1_N
39	TRC_CPU0_PTI010	54	TRC_CPU0_PTI114
40	TRC_CPU0_PTI19	55	DBP_CPU0_HOOK8_MBP2_QS_R1_N
41	TRC_CPU0_PTI011	56	TRC_CPU0_PTI115
42	PWRGD_CPU0_LVC1_MIPI60	57	GND
43	TRC_CPU0_PTI012	58	GND
44	TRC_CPU0_PTI110	59	TRC_CPU0_PTI0_CLK1
45	TRC_CPU0_PTI013	60	TRC_CPU0_PTI1_CLK1

XDP Debug Connector (For CPU2)

Connector type: 2x30 60-pin header
Connector location: CN15

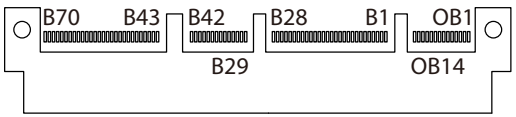


Pin	Definition	Pin	Definition
1	PD_CPU1_DBP_PIN1	16	GND
2	NC	17	GND
3	NC	18	TRC_CPU1_PTI10
4	NC	19	TRC_CPU1_PTI00
5	NC	20	TRC_CPU1_PTI11
6	NC	21	TRC_CPU1_PTI01
7	NC	22	TRC_CPU1_PTI12
8	PD_TRST_CPU1	23	TRC_CPU1_PTI02
9	NC	24	TRC_CPU1_PTI13
10	NC	25	TRC_CPU1_PTI03
11	NC	26	TRC_CPU1_PTI14
12	PVNN_TERM_CPU1	27	TRC_CPU1_PTI04
13	TRC_CPU1_PTI0_CLK0	28	TRC_CPU1_PTI15
14	TRC_CPU1_PTI1_CLK0	29	TRC_CPU1_PTI05
15	GND	30	TRC_CPU1_PTI16

Pin	Definition	Pin	Definition
31	TRC_CPU1_PTI06	46	TRC_CPU1_PTI111
32	TRC_CPU1_PTI17	47	TRC_CPU1_PTI014
33	TRC_CPU1_PTI07	48	TRC_CPU1_PTI112
34		49	TRC_CPU1_PTI015
35	TRC_CPU1_PTI08	50	TRC_CPU1_PTI113
36		51	
37	TRC_CPU1_PTI09	52	P3V3_AUX
38	TRC_CPU1_PTI18	53	DBP_CPU1_HOOK9_MBP3_QS_R1_N
39	TRC_CPU1_PTI010	54	TRC_CPU1_PTI114
40	TRC_CPU1_PTI19	55	DBP_CPU1_HOOK8_MBP2_QS_R1_N
41	TRC_CPU1_PTI011	56	TRC_CPU1_PTI115
42	PWRGD_CPU1_LVC1_MIPI60	57	GND
43	TRC_CPU1_PTI012	58	GND
44	TRC_CPU1_PTI110	59	TRC_CPU1_PTI0_CLK1
45	TRC_CPU1_PTI013	60	TRC_CPU1_PTI1_CLK1

IO Slot Connector

Connector type: 2x84 168-pin header
Connector location: CN9, CN14, CN17, CN20



Pin	Definition	Pin	Definition
OA1	PE_SLOT_RST2_N	OB1	NO USE
OA2	PE_SLOT_RST3_N	OB2	NO USE
OA3	IRQ_LVC3_WAKE_N	OB3	NO USE
OA4	NO USE	OB4	NC
OA5	NO USE	OB5	NO USE
OA6	NO USE	OB6	NO USE
OA7	NO USE	OB7	NO USE
OA8	NO USE	OB8	NO USE
OA9	NO USE	OB9	NO USE
OA10	GND	OB10	GND
OA11	PE_SLOT_CLK3_DN	OB11	PE_SLOT_CLK2_DN
OA12	PE_SLOT_CLK3_DP	OB12	PE_SLOT_CLK2_DP
OA13	GND	OB13	GND
OA14	NO USE	OB14	NO USE

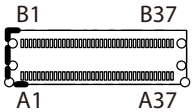
Pin	Definition	Pin	Definition
A1	GND	B1	P12V
A2	GND	B2	P12V
A3	GND	B3	P12V
A4	GND	B4	P12V
A5	GND	B5	P12V
A6	GND	B6	P12V
A7	SLOT_R_SCL	B7	NO USE
A8	SLOT_R_SDA	B8	NO USE
A9	NO USE	B9	NO USE
A10	GND	B10	PE_SLOT_RST0_N
A11	PE_SLOT_RST1_N	B11	P3V3_SLOT
A12	NO USE	B12	NO USE
A13	GND	B13	GND
A14	PE_SLOT_CLK1_DN	B14	PE_SLOT_CLK0_DN
A15	PE_SLOT_CLK1_DP	B15	PE_SLOT_CLK0_DP

Pin	Definition	Pin	Definition
A16	GND	B16	GND
A17	PE_SLOT_RX_DN0	B17	PE_SLOT_TX_C_DN0
A18	PE_SLOT_RX_DP0	B18	PE_SLOT_TX_C_DP0
A19	GND	B19	GND
A20	PE_SLOT_RX_DN1	B20	PE_SLOT_TX_C_DN1
A21	PE_SLOT_RX_DP1	B21	PE_SLOT_TX_C_DP1
A22	GND	B22	GND
A23	PE_SLOT_RX_DN2	B23	PE_SLOT_TX_C_DN2
A24	PE_SLOT_RX_DP2	B24	PE_SLOT_TX_C_DP2
A25	GND	B25	GND
A26	PE_SLOT_RX_DN3	B26	PE_SLOT_TX_C_DN3
A27	PE_SLOT_RX_DP3	B27	PE_SLOT_TX_C_DP3
A28	GND	B28	GND
A29	GND	B29	GND
A30	PE_SLOT_RX_DN4	B30	PE_SLOT_TX_C_DN4
A31	PE_SLOT_RX_DP4	B31	PE_SLOT_TX_C_DP4
A32	GND	B32	GND
A33	PE_SLOT_RX_DN5	B33	PE_SLOT_TX_C_DN5
A34	PE_SLOT_RX_DP5	B34	PE_SLOT_TX_C_DP5
A35	GND	B35	GND
A36	PE_SLOT_RX_DN6	B36	PE_SLOT_TX_C_DN6
A37	PE_SLOT_RX_DP6	B37	PE_SLOT_TX_C_DP6
A38	GND	B38	GND
A39	PE_SLOT_RX_DN7	B39	PE_SLOT_TX_C_DN7
A40	PE_SLOT_RX_DP7	B40	PE_SLOT_TX_C_DP7
A41	GND	B41	GND
A42	NO USE	B42	NO USE
A43	GND	B43	GND

Pin	Definition	Pin	Definition
A44	PE_SLOT_RX_DN8	B44	PE_SLOT_TX_C_DN8
A45	PE_SLOT_RX_DP8	B45	PE_SLOT_TX_C_DP8
A46	GND	B46	GND
A47	PE_SLOT_RX_DN9	B47	PE_SLOT_TX_C_DN9
A48	PE_SLOT_RX_DP9	B48	PE_SLOT_TX_C_DP9
A49	GND	B49	GND
A50	PE_SLOT_RX_DN10	B50	PE_SLOT_TX_C_DN10
A51	PE_SLOT_RX_DP10	B51	PE_SLOT_TX_C_DP10
A52	GND	B52	GND
A53	PE_SLOT_RX_DN11	B53	PE_SLOT_TX_C_DN11
A54	PE_SLOT_RX_DP11	B54	PE_SLOT_TX_C_DP11
A55	GND	B55	GND
A56	PE_SLOT_RX_DN12	B56	PE_SLOT_TX_C_DN12
A57	PE_SLOT_RX_DP12	B57	PE_SLOT_TX_C_DP12
A58	GND	B58	GND
A59	PE_SLOT_RX_DN13	B59	PE_SLOT_TX_C_DN13
A60	PE_SLOT_RX_DP13	B60	PE_SLOT_TX_C_DP13
A61	GND	B61	GND
A62	PE_SLOT_RX_DN14	B62	PE_SLOT_TX_C_DN14
A63	PE_SLOT_RX_DP14	B63	PE_SLOT_TX_C_DP14
A64	GND	B64	GND
A65	PE_SLOT_RX_DN15	B65	PE_SLOT_TX_C_DN15
A66	PE_SLOT_RX_DP15	B66	PE_SLOT_TX_C_DP15
A67	GND	B67	GND
A68		B68	
A69		B69	
A70	NO USE	B70	NO USE

MCIO Connector

Connector type: 2X37 74-Pin
Connector location: CN10, CN13, CN16, CN18

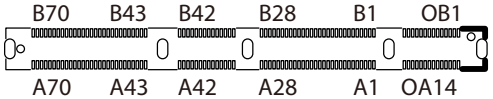


Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE_SLOT_RX_DP0	B2	PE_SLOT_TX_C_DP0
A3	PE_SLOT_RX_DN0	B3	PE_SLOT_TX_C_DN0
A4	GND	B4	GND
A5	PE_SLOT_RX_DP1	B5	PE_SLOT_TX_C_DP1
A6	PE_SLOT_RX_DN1	B6	PE_SLOT_TX_C_DN1
A7	GND	B7	GND
A8	NC	B8	NC
A9	NC	B9	NC
A10	GND	B10	GND
A11	NC	B11	NC
A12	NC	B12	NC
A13	GND	B13	GND
A14	PE_SLOT_RX_DP2	B14	PE_SLOT_TX_C_DP2
A15	PE_SLOT_RX_DN2	B15	PE_SLOT_TX_C_DN2
A16	GND	B16	GND
A17	PE_SLOT_RX_DP3	B17	PE_SLOT_TX_C_DP3
A18	PE_SLOT_RX_DN3	B18	PE_SLOT_TX_C_DN3

Pin	Definition	Pin	Definition
A19	GND	B19	GND
A20	PE_SLOT_RX_DP4	B20	PE_SLOT_TX_C_DP4
A21	PE_SLOT_RX_DN4	B21	PE_SLOT_TX_C_DN4
A22	GND	B22	GND
A23	PE_SLOT_RX_DP5	B23	PE_SLOT_TX_C_DP5
A24	PE_SLOT_RX_DN5	B24	PE_SLOT_TX_C_DN5
A25	GND	B25	GND
A26	NC	B26	NC
A27	NC	B27	NC
A28	GND	B28	GND
A29	NC	B29	NC
A30	NC	B30	NC
A31	GND	B31	GND
A32	PE_SLOT_RX_DP6	B32	PE_SLOT_TX_C_DP6
A33	PE_SLOT_RX_DN6	B33	PE_SLOT_TX_C_DN6
A34	GND	B34	GND
A35	PE_SLOT_RX_DP7	B35	PE_SLOT_TX_C_DP7
A36	PE_SLOT_RX_DN7	B36	PE_SLOT_TX_C_DN7
A37	GND	B37	GND

Riser Left Connector

Connector type: 2x70 140-pin header
Connector location: CN12



Pin	Definition	Pin	Definition
OA1	NC	OB1	PE_SLOT3_NIC_PWR_GOOD
OA2	NC	OB2	MAIN_PWR_EN_SLOT
OA3	FM_LAN_WAKE_SLOT3_N	OB3	PE_SLOT4_NIC_PWR_GOOD_R
OA4	GND	OB4	PE_SLOT4_R_PRSNTB0#
OA5	PE_SLOT4_CLK_RETIMER_DN	OB5	PE_SLOT4_R_PRSNTB1#
OA6	PE_SLOT4_CLK_RETIMER_DP	OB6	PE_SLOT4_R_PRSNTB2#
OA7	GND	OB7	GND
OA8	SLOT4_R2_SCL	OB8	PE_SLOT3_CLK_RETIMER_DN
OA9	SLOT4_R2_SDA	OB9	PE_SLOT3_CLK_RETIMER_DP
OA10	GND	OB10	GND

Note that the definition on this connector is not the standard pin definition of an OCP connector.

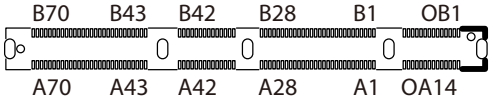
Pin	Definition	Pin	Definition
OA11	PE_SLOT4_CLK1_DN	OB11	PE_SLOT4_CLK0_DN
OA12	PE_SLOT4_CLK1_DP	OB12	PE_SLOT4_CLK0_DP
OA13	GND	OB13	GND
OA14	NC	OB14	PE_SLOT4_R_PRSNTB3#
A1	GND	B1	P3V3
A2	GND	B2	P3V3
A3	GND	B3	P3V3
A4	GND	B4	P3V3
A5	GND	B5	P3V3
A6	GND	B6	P3V3
A7	SLOT3_R2_SCL	B7	P3V3_AUX
A8	SLOT3_R2_SDA	B8	NC
A9	RST_SMB_HOST_MUX_PE_BUFF_N	B9	NC
A10	GND	B10	PE_SLOT34_RST_N
A11	NC	B11	P3V3_AUX

Pin	Definition	Pin	Definition
A12	PE_SLOT3_PRSNTB2#	B12	AUX_PWR_EN_SLOT
A13	GND	B13	GND
A14	PE_SLOT3_CLK1_DN	B14	PE_SLOT3_CLK0_DN
A15	PE_SLOT3_CLK1_DP	B15	PE_SLOT3_CLK0_DP
A16	GND	B16	GND
A17	PE_SLOT3_RX_DP15	B17	PE_SLOT3_TX_DP15
A18	PE_SLOT3_RX_DN15	B18	PE_SLOT3_TX_DN15
A19	GND	B19	GND
A20	PE_SLOT3_RX_DP14	B20	PE_SLOT3_TX_DP14
A21	PE_SLOT3_RX_DN14	B21	PE_SLOT3_TX_DN14
A22	GND	B22	GND
A23	PE_SLOT3_RX_DP13	B23	PE_SLOT3_TX_DP13
A24	PE_SLOT3_RX_DN13	B24	PE_SLOT3_TX_DN13
A25	GND	B25	GND
A26	PE_SLOT3_RX_DP12	B26	PE_SLOT3_TX_DP12
A27	PE_SLOT3_RX_DN12	B27	PE_SLOT3_TX_DN12
A28	GND	B28	GND
A29	GND	B29	GND
A30	PE_SLOT3_RX_DP11	B30	PE_SLOT3_TX_DP11
A31	PE_SLOT3_RX_DN11	B31	PE_SLOT3_TX_DN11
A32	GND	B32	GND
A33	PE_SLOT3_RX_DP10	B33	PE_SLOT3_TX_DP10
A34	PE_SLOT3_RX_DN10	B34	PE_SLOT3_TX_DN10
A35	GND	B35	GND
A36	PE_SLOT3_RX_DP9	B36	PE_SLOT3_TX_DP9
A37	PE_SLOT3_RX_DN9	B37	PE_SLOT3_TX_DN9
A38	GND	B38	GND
A39	PE_SLOT3_RX_DP8	B39	PE_SLOT3_TX_DP8
A40	PE_SLOT3_RX_DN8	B40	PE_SLOT3_TX_DN8
A41	GND	B41	GND

Pin	Definition	Pin	Definition
A42	PE_SLOT3_PRSNTB1#	B42	PE_SLOT3_PRSNTB0#
A43	GND	B43	GND
A44	PE_SLOT3_RX_DP7	B44	PE_SLOT3_TX_DP7
A45	PE_SLOT3_RX_DN7	B45	PE_SLOT3_TX_DN7
A46	GND	B46	GND
A47	PE_SLOT3_RX_DP6	B47	PE_SLOT3_TX_DP6
A48	PE_SLOT3_RX_DN6	B48	PE_SLOT3_TX_DN6
A49	GND	B49	GND
A50	PE_SLOT3_RX_DP5	B50	PE_SLOT3_TX_DP5
A51	PE_SLOT3_RX_DN5	B51	PE_SLOT3_TX_DN5
A52	GND	B52	GND
A53	PE_SLOT3_RX_DP4	B53	PE_SLOT3_TX_DP4
A54	PE_SLOT3_RX_DN4	B54	PE_SLOT3_TX_DN4
A55	GND	B55	GND
A56	PE_SLOT3_RX_DP3	B56	PE_SLOT3_TX_DP3
A57	PE_SLOT3_RX_DN3	B57	PE_SLOT3_TX_DN3
A58	GND	B58	GND
A59	PE_SLOT3_RX_DP2	B59	PE_SLOT3_TX_DP2
A60	PE_SLOT3_RX_DN2	B60	PE_SLOT3_TX_DN2
A61	GND	B61	GND
A62	PE_SLOT3_RX_DP1	B62	PE_SLOT3_TX_DP1
A63	PE_SLOT3_RX_DN1	B63	PE_SLOT3_TX_DN1
A64	GND	B64	GND
A65	PE_SLOT3_RX_DP0	B65	PE_SLOT3_TX_DP0
A66	PE_SLOT3_RX_DN0	B66	PE_SLOT3_TX_DN0
A67	GND	B67	GND
A68	NC	B68	NC
A69	NC	B69	NC
A70	PE_SLOT34_PWRBRK0#	B70	PE_SLOT3_PRSNTB3#

Riser Right Connector

Connector type: 2x70 140-pin header
Connector location: CN21



Pin	Definition	Pin	Definition
OA1	PE_SLOT7_R_PRSNTB0#	OB1	PE_SLOT8_NIC_PWR_GOOD
OA2	PE_SLOT7_R_PRSNTB1#	OB2	MAIN_PWR_EN_SLOT
OA3	FM_LAN_WAKE_SLOT78_N	OB3	PE_SLOT7_NIC_PWR_GOOD_R
OA4	PE_SLOT7_R_PRSNTB2#	OB4	NC
OA5	PE_SLOT7_R_PRSNTB3#	OB5	SLOT7_R2_SCL
OA6	NC	OB6	SLOT7_R2_SDA
OA7	GND	OB7	GND
OA8	PE_SLOT78_CLK_RETIMER_DN	OB8	PE_SLOT9_CLK0_DN
OA9	PE_SLOT78_CLK_RETIMER_DP	OB9	PE_SLOT9_CLK0_DP
OA10	GND	OB10	GND

Note that the definition on this connector is not the standard pin definition of an OCP connector.

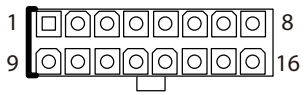
Pin	Definition	Pin	Definition
OA11	PE_SLOT7_CLK1_DN	OB11	PE_SLOT7_CLK0_DN
OA12	PE_SLOT7_CLK1_DP	OB12	PE_SLOT7_CLK0_DP
OA13	GND	OB13	GND
OA14	NC	OB14	PE_SLOT9_PWRBRK0#
A1	GND	B1	P3V3
A2	GND	B2	P3V3
A3	GND	B3	P3V3
A4	GND	B4	P3V3
A5	GND	B5	P3V3
A6	GND	B6	P3V3
A7	SLOT8_EXPANSION_R2_SCL	B7	P3V3_AUX
A8	SLOT8_EXPANSION_R2_SDA	B8	RETIMER_CPLD_SMB_SCL_R2
A9	RST_SMB_HOST_MUX_PE_BUFF_N	B9	RETIMER_CPLD_SMB_SDA_R2
A10	GND	B10	PE_SLOT78_RST_N
A11	PE_EXPANSION_RST_N	B11	P3V3_AUX

Pin	Definition	Pin	Definition
A12	PE_SLOT8_R_PRSNTB2#	B12	AUX_PWR_EN_SLOT
A13	GND	B13	GND
A14	PE_SLOT8_CLK1_DN	B14	PE_SLOT8_CLK0_DN
A15	PE_SLOT8_CLK1_DP	B15	PE_SLOT8_CLK0_DP
A16	GND	B16	GND
A17	PE_SLOT8_RX_DP7	B17	PE_SLOT8_TX_DP7
A18	PE_SLOT8_RX_DN7	B18	PE_SLOT8_TX_DN7
A19	GND	B19	GND
A20	PE_SLOT8_RX_DP6	B20	PE_SLOT8_TX_DP6
A21	PE_SLOT8_RX_DN6	B21	PE_SLOT8_TX_DN6
A22	GND	B22	GND
A23	PE_SLOT8_RX_DP5	B23	PE_SLOT8_TX_DP5
A24	PE_SLOT8_RX_DN5	B24	PE_SLOT8_TX_DN5
A25	GND	B25	GND
A26	PE_SLOT8_RX_DP4	B26	PE_SLOT8_TX_DP4
A27	PE_SLOT8_RX_DN4	B27	PE_SLOT8_TX_DN4
A28	GND	B28	GND
A29	GND	B29	GND
A30	PE_SLOT8_RX_DP3	B30	PE_SLOT8_TX_DP3
A31	PE_SLOT8_RX_DN3	B31	PE_SLOT8_TX_DN3
A32	GND	B32	GND
A33	PE_SLOT8_RX_DP2	B33	PE_SLOT8_TX_DP2
A34	PE_SLOT8_RX_DN2	B34	PE_SLOT8_TX_DN2
A35	GND	B35	GND
A36	PE_SLOT8_RX_DP1	B36	PE_SLOT8_TX_DP1
A37	PE_SLOT8_RX_DN1	B37	PE_SLOT8_TX_DN1
A38	GND	B38	GND
A39	PE_SLOT8_RX_DP0	B39	PE_SLOT8_TX_DP0
A40	PE_SLOT8_RX_DN0	B40	PE_SLOT8_TX_DN0
A41	GND	B41	GND

Pin	Definition	Pin	Definition
A42	PE_SLOT8_R_PRSNTB1#	B42	PE_SLOT8_R_PRSNTB0#
A43	GND	B43	GND
A44	PE_SLOT7_RX_DP7	B44	PE_SLOT7_TX_DP7
A45	PE_SLOT7_RX_DN7	B45	PE_SLOT7_TX_DN7
A46	GND	B46	GND
A47	PE_SLOT7_RX_DP6	B47	PE_SLOT7_TX_DP6
A48	PE_SLOT7_RX_DN6	B48	PE_SLOT7_TX_DN6
A49	GND	B49	GND
A50	PE_SLOT7_RX_DP5	B50	PE_SLOT7_TX_DP5
A51	PE_SLOT7_RX_DN5	B51	PE_SLOT7_TX_DN5
A52	GND	B52	GND
A53	PE_SLOT7_RX_DP4	B53	PE_SLOT7_TX_DP4
A54	PE_SLOT7_RX_DN4	B54	PE_SLOT7_TX_DN4
A55	GND	B55	GND
A56	PE_SLOT7_RX_DP3	B56	PE_SLOT7_TX_DP3
A57	PE_SLOT7_RX_DN3	B57	PE_SLOT7_TX_DN3
A58	GND	B58	GND
A59	PE_SLOT7_RX_DP2	B59	PE_SLOT7_TX_DP2
A60	PE_SLOT7_RX_DN2	B60	PE_SLOT7_TX_DN2
A61	GND	B61	GND
A62	PE_SLOT7_RX_DP1	B62	PE_SLOT7_TX_DP1
A63	PE_SLOT7_RX_DN1	B63	PE_SLOT7_TX_DN1
A64	GND	B64	GND
A65	PE_SLOT7_RX_DP0	B65	PE_SLOT7_TX_DP0
A66	PE_SLOT7_RX_DN0	B66	PE_SLOT7_TX_DN0
A67	GND	B67	GND
A68	NC	B68	NC
A69	NC	B69	NC
A70	PE_SLOT78_PWRBRK0#	B70	PE_SLOT8_R_PRSNTB3#

Power Connector (Internal Cable Use CON1 to CON2)

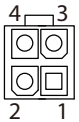
Connector type: 2X8 16-Pin
Connector location: CON1, CON2



Pin	Definition	Pin	Definition
1	P12V_CPU	9	P12V_CPU
2	P12V_CPU	10	P12V_CPU
3	P12V_CPU	11	P12V_CPU
4	P12V_CPU	12	P12V_CPU
5	P12V_CPU	13	P12V_CPU
6	P12V_CPU	14	P12V_CPU
7	P12V_CPU	15	P12V_CPU
8	P12V_CPU	16	P12V_CPU

Power Connector Connector (Internal Cable Use CON1 to CON2)

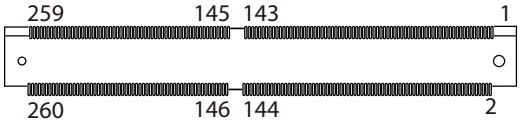
Connector type: 2X2 4-Pin
Connector location: CON3, CON4



Pin	Definition
1	P12V_CPU1
2	P12V_CPU1
3	P12V_S3_AUX_CPU1
4	P12V_S3_AUX_CPU1

Run BMC Connector

Connector type: 260-pin header
Connector location: DIMM1



Pin	Definition	Pin	Definition
1	P12V_AUX	2	NC
3	P3V3_BMC	4	P3V3_BMC
5	P3V3_BMC	6	P3V3_BMC
7	P3V3_BMC	8	GND
9	GND	10	V_BMC_GFX_REAR_GRN
11	GND	12	V_BMC_GFX_REAR_BLU
13	SGPIO_BMC_LD_R_N	14	V_BMC_GFX_REAR_RED
15	SGPIO_BMC_DIN	16	V_BMC_GFX_REAR_HSYN
17	SGPIO_BMC_DOUT	18	V_BMC_GFX_REAR_VSYN
19	SGPIO_BMC_CLK_R	20	SMB_BMC_DDC_SCL_R
21	BMC_RXD5	22	SMB_BMC_DDC_SDA_R
23	BMC_TXD5	24	GND
25	FP_ID_LED_R_N	26	BMC_FAN1_PWM
27	BMC_FAN3_PWM	28	BMC_FAN2_PWM
29	BMC_FAN5_PWM	30	BMC_FAN4_PWM

Pin	Definition	Pin	Definition
31	IRQ_BMC_CPU_NMI_R	32	BMC_FAN6_PWM
33	RNBMC_R1_PRSNT#	34	CPLD_BMC_SMI_R#
35	IRQ_BMC_PCH_SMI_LPC_N_BMC	36	BMC_GPIO19
37	FM_P1V2_BMC_AUX_EN_R	38	BMC_CPLD_UART1_R_CTS#
39	GND	40	BMC_CPLD_UART1_R_NDCD
41	BMC_CPLD_UART1_R_RXD	42	ID_LED_BMC_OUT
43	BMC_CPLD_UART1_R_TXD	44	BMC_GPIO24
45	GND	46	BMC_CPLD_UART1_R_NDSR
47	SMB_CPLD_STBY_LVC3_MM8_R3_CLK	48	SMB_CPU_PIROM_BMC_SCL
49	SMB_CPLD_STBY_LVC3_MM8_R3_DATA	50	SMB_CPU_PIROM_BMC_SDA
51	GND	52	GND
53	SMB_SENSOR_STBY_LVC3_R1_CLK	54	SMB_SMLINK0_STBY_LVC3_R2_SCL

Pin	Definition	Pin	Definition
55	SMB_SENSOR_STBY_LVC3_R1_DATA	56	SMB_SMLINK0_STBY_LVC3_R2_SDA
57	GND	58	GND
59	FM_CPU_ERR0_LVT3_BMC_N	60	SMB_BMC_STBY_LVC3_MM5_R_CLK
61	FM_CPU_ERR1_LVT3_BMC_N	62	SMB_BMC_STBY_LVC3_MM5_R_DATA
63	SPI_BMC_BOOT_CS0_R_N	64	GND
65	SPI_BMC_BOOT_R_MOSI	66	BMC_CPLD_UART1_R_RI
67	SPI_BMC_BOOT_R_MISO	68	BMC_CPLD_UART1_R_DTR
69	SPI_BMC_BOOT_R_IO2	70	BMC_CPLD_UART1_R_RTS#
71	SPI_BMC_BOOT_R_IO3	72	FP_LED_STATUS_GREEN_R_N
73	SPI_BMC_BOOT_R_CLK	74	FM_BIOS_POST_CMPLT_BMC_N
75	SPI_BMC_BOOT_CS1_R_N	76	IRQ_BMC_PCH_NMI_R
77	PWRGD_BMC_PS_PWROK_R	78	BMC_FAN1_TACH
79	FM_BMC_CRASHLOG_TRIG_N_BMC	80	BMC_FAN2_TACH
81	FM_CPU1_SKTOCC_LVT3_R1_N	82	BMC_FAN3_TACH
83	BMC_GPIO49	84	BMC_FAN4_TACH
85	FM_CPU_CATERR_R2_N	86	BMC_FAN5_TACH
87	RST_PFR_EXTRST_N	88	BMC_FAN6_TACH
89	FM_BMC_PCH_SCI_LPC_R2_N	90	FM_SLPS3_R_N
91	FM_PCHHOT_N_BMC	92	FM_SLPS4_R_N
93	FM_PLT_BMC_THERMTRIP_N_BMC	94	CRPS_BMC_PRESEND1
95	A_VBAT_DETECT	96	FM_BMC_PCH_SPARE_R2
97	RST_CPU0_LVC1_N_BMC	98	I3C_SPD_DDRABCD_CPU0_BMC_R2_SCL

Pin	Definition	Pin	Definition
99	PWRGD_P1V2_BMC_AUX_R	100	I3C_SPD_DDRABCD_CPU0_BMC_R2_SDA
101	GPIOH1_CPLD_BMC_R	102	I3C_SPD_DDREFGH_CPU0_BMC_R2_SCL
103	FM_PFR_ACTIVE_N_BMC	104	I3C_SPD_DDREFGH_CPU0_BMC_R2_SDA
105	IRQ_SML1_PMBUS_BMC_ALERT_R2_N	106	I3C_SPD_DDRABCD_CPU1_BMC_R2_SCL
107	JTAG_SEL_BMC	108	I3C_SPD_DDRABCD_CPU1_BMC_R2_SDA
109	BMC_GPIO114	110	GND
111	PVNN_TERM_CPU0	112	PECI_BMC_R
113	GPIOAA0	114	GND
115	IRQ_SML0_ALERT_BMC_N	116	CRPS_BMC_PRESEND2
117	FM_SPD_SWITCH_CTRL_N_BMC	118	FM_P2V5_BMC_EN
119	FM_CPU1_DISABLE_COD_N	120	I3C_SPD_DDREFGH_CPU1_BMC_R2_SCL
121	BMC_GPIO83	122	I3C_SPD_DDREFGH_CPU1_BMC_R2_SDA
123	SMB_IPMB_STBY_LVC3_CLK	124	BMC_GPIO86
125	SMB_IPMB_STBY_LVC3_DATA	126	GND
127	GND	128	SMB_BMC_SPD_ACCESS_STBY_LVC3_SCL_R1
129	GPIOH0_CPLD_BMC_R	130	SMB_BMC_SPD_ACCESS_STBY_LVC3_SDA_R1
131	BMC_READY	132	GND
133	GND	134	SMB_PMBUS_BMC_STBY_LVC3_R4_SCL
135	IRQ_SMI_ACTIVE_BMC_R_N	136	SMB_PMBUS_BMC_STBY_LVC3_R4_SDA
137	IRQ_NMI_EVENT_BMC_N	138	FP_LED_STATUS_AMBER_R_N

Pin	Definition	Pin	Definition
139	GND	140	H_CPU0_MEMHOT_OUT_LVC1_BMC_N
141	FP_SYS_RESET_R1_N	142	RST_PLTRST_B_N
143	RST_BTN_BMC_N	144	BMC_GPIO100
145	GND	146	BMC_GPIO101
147	PE_BMC_TXN	148	□NC
149	PE_BMC_TXP	150	□NC
151	GND	152	PGPPA_AUX
153	PCIE_RX_BMC_DN	154	FM_CPU1_MEMHOT_OUT_BMC_N
155	PCIE_RX_BMC_DP	156	FM_BMC_ONCTL_N_PLD_R
157	GND	158	BMC_GPIO106
159	CLK_100M_GEN3_BMC_PE_DN	160	DBP_PRESENT_IN_R2_N
161	CLK_100M_GEN3_BMC_PE_DP	162	BMCJTAG1TRST
163	GND	164	JTAG_TDO_BMC
165	RST_LPC_LRST_ESPI_RST_BMC_R_N	166	JTAG_TDI_BMC
167	ESPI_IO1_LPC_LAD1_R	168	BMC_JTAG1RTCK
169	ESPI_IO0_LPC_LAD0_R	170	JTAG_TCK_BMC
171	IRQ_LPC_SERIRQ_ESPI_ALERT_N_BMC	172	JTAG_TMS_BMC
173	ESPI_CS1_N_LFRAME_N_BMC	174	A_P12V_SCALED
175	ESPI_IO3_LPC_LAD3_R	176	A_P3V3_SCALED
177	ESPI_IO2_LPC_LAD2_R	178	A_P5V_SCALED
179	PCICLK_BMC	180	A_P1V05_PCH_AUX_SCALED
181	BMC_I2C9SCL_R	182	A_PVNN_PCH_AUX_SCALED
183	BMC_I2C9SDA_R	184	A_VCC_CPU0_SCALED
185	GND	186	A_VCC_CPU1_SCALED
187	PWRGD_PCH_PWROK_R2	188	PVCCFA_EHV_FIVRA_CPU0_SCALED

Pin	Definition	Pin	Definition
189	FM_CPU0_SKTOCC_LVT3_R1_N	190	SPI_PFR_PCH_RNBMC_CS0_N
191	GND	192	BMC_GPO1
193	FM_CPU_ERR2_LVT3_BMC_N	194	BMC_GPO2
195	AC_FAIL_PSU_BMC	196	BMC_GPIO16
197	GND	198	SPI_IBMC_SSB_CS0_N
199	FP_BMC_PWR_BTN_R_N	200	SPI_BMC_MUXED_BIOS_IO0_R
201	PWR_BTN_BMC_N	202	SPI_BMC_MUXED_BIOS_IO1_R
203	GND	204	SPI_BMC_MUXED_BIOS_IO2_R
205	BMC_I2C03SCL	206	SPI_BMC_MUXED_BIOS_IO3_R
207	BMC_I2C03SDA	208	SPI_BMC_MUXED_BIOS_CLK_R
209	FP_ID_BTN_PFR_BMC_N	210	SPI_IBMC_SSB_CS1_N
211	PWRGD_P2V5_BMC_AUX_R	212	GND
213	FM_P1V0_BMC_AUX_EN_R	214	RMIIMDIO
215	GND	216	NCSI_CRS_DV_A
217	USB2_P10_DN	218	RMIIMDC
219	USB2_P10_DP	220	NCSI_IBMC_CLK_A
221	GND	222	BMC_RMIIRXER
223	USB2_P12_BMC_DN	224	NCSI_TX_EN_A
225	USB2_P12_BMC_DP	226	GND
227	GND	228	NCSI_RXD0_A
229	NCSI_TXD0_B	230	NCSI_RXD1_A
231	NCSI_RXD0_B	232	GND
233	GND	234	NCSI_TXD0_A
235	NCSI_RXD1_B	236	NCSI_TXD1_A
237	NCSI_TXD1_B	238	GND

Pin	Definition	Pin	Definition
239	GND	240	NCSI_TXCLK_B
241	NCSI_CRS_DV_B	242	PHYLED2_RGMIIRXCTL
243	NCSI_RXD2_B	244	NCSI_TXCTL_B
245	GND	246	FM_BMC_BMCINIT_R
247	TRD3N_RGMIIRXD3	248	BMC_AUX_PWRGD_R2
249	NCSI_TXD3_B	250	NCSI_IBMC_CLK_B
251	GND	252	PVCCFA_EHV_FIVRA_CPU1_SCALED
253	RST_SRST_BMC_PLD_N	254	A_PVCCFA_EHV_CPU1_SCALED
255	A_P3V_BAT_SCALED	256	A_PVCCFA_EHV_CPU0_SCALED
257	A_PVCCINFAON_CPU1_SCALED	258	A_PVCCINFAON_CPU0_SCALED
259	GPI7_ADC15	260	GPI6_ADC14

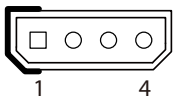
SYS RTC Header

Connector type: 1X2 2-Pin
Connector location: J1

Pin	Definition
1	GND
2	3V3_BAT

SATA Power Connector

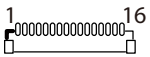
Connector type: 1X4 4-Pin
Connector location: J2



Pin	Definition
1	P12V
2	GND
3	GND
4	P5V

VGA Connector

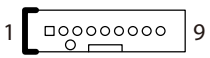
Connector type: 1x16 16-pin header
Connector location: J3



Pin	Definition	Pin	Definition
1	VGA_VCC	9	V_BMC_GFX_REAR_HSYN_R3
2	GND	10	NC
3	NC	11	GND
4	SMB_BMC_DDC_SCL_R1	12	V_BMC_GFX_REAR_BLU_R1
5	SMB_BMC_DDC_SDA_R1	13	GND
6	NC	14	V_BMC_GFX_REAR_GRN_R1
7	V_BMC_GFX_REAR_VSYN_R3	15	GND
8	GND	16	V_BMC_GFX_REAR_RED_R1

Fan Wafer Connector

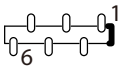
Connector type: 1X9 9-Pin
Connector location: J10, J11, J12



Pin	Definition
1	P12V
2	P12V
3	TACH FRONT
4	TACH REAR
5	N/C
6	PWM REAR
7	PWM FRONT
8	GND
9	GND

CPLD JTAG for Programing CPLD CODE

Connector type: 1X6 6-Pin
Connector location: JP11



Pin	Definition
1	P3V3_CPLD
2	GND
3	JTAG_TCK_CPLD
4	JTAG_TDO_CPLD
5	JTAG_TDI_CPLD
6	JTAG_TMS_CPLD

Header to BTN Switch with Cable

Connector type: 2X1 2-Pin
Connector location: JP17

Pin	Definition
1	PWRBTN_N
2	GND

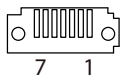
Header to LED with Cable

Connector type: 2X1 2-Pin
Connector location: JP18

Pin	Definition
1	P3V3_CPLD
2	ID_LED_N

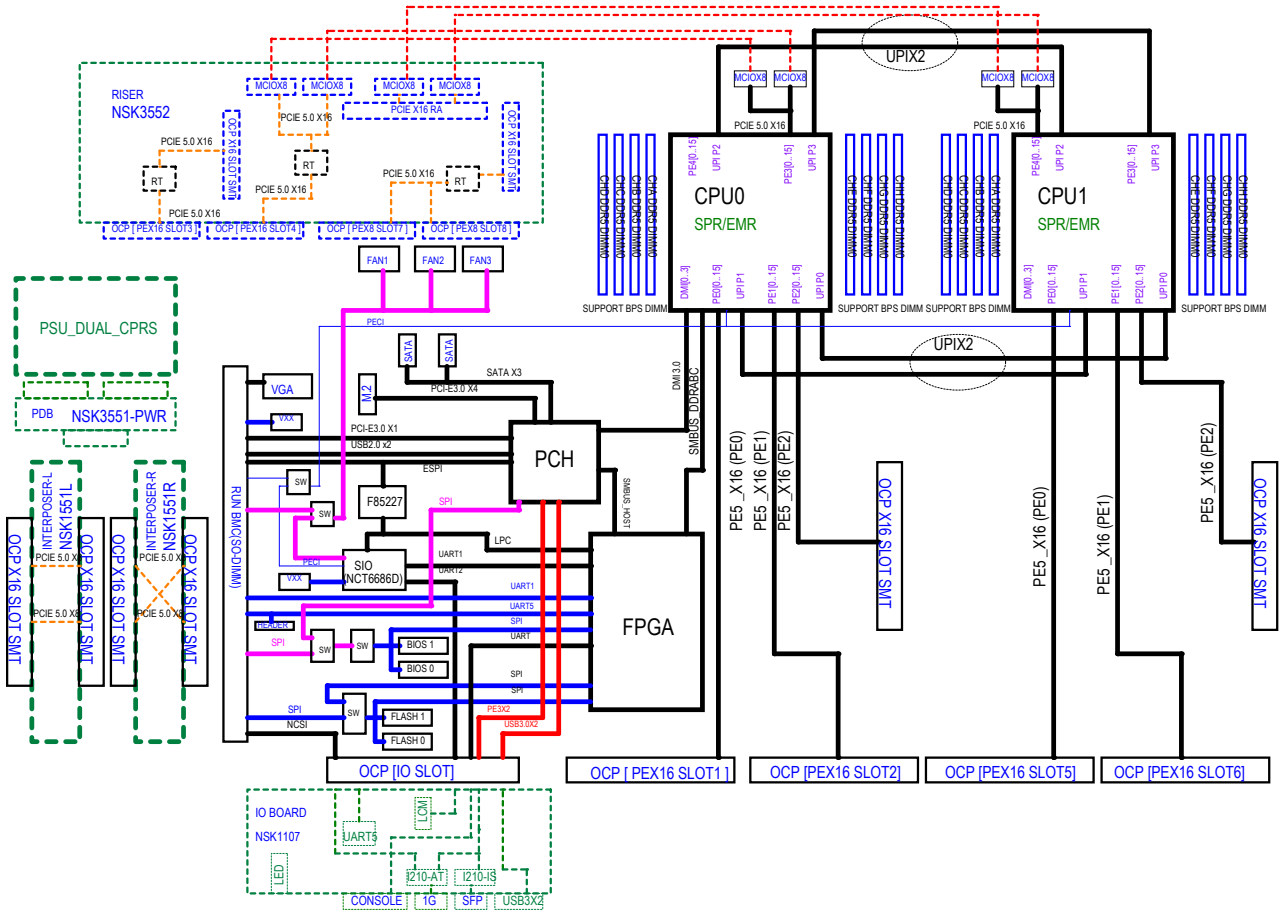
SATA Connector

Connector type: 1X7 7-Pin
Connector location: SATA1, SATA2



Pin	Definition	Pin	Definition
1	GND	2	TXP
4	GND	3	TXN
7	GND	5	RXN
		6	RXP

Block Diagram



Chapter 3: System Setup

Removing the Chassis Cover

Prior to removing the chassis cover, make sure the unit's power is off and disconnected from the power sources for 20 seconds to prevent electric shock or system damage.

1. The screws on the top and sides are used to secure the cover to the chassis. Remove these screws and put them in a safe place for later use.

Screws on the sides

Screws on the top

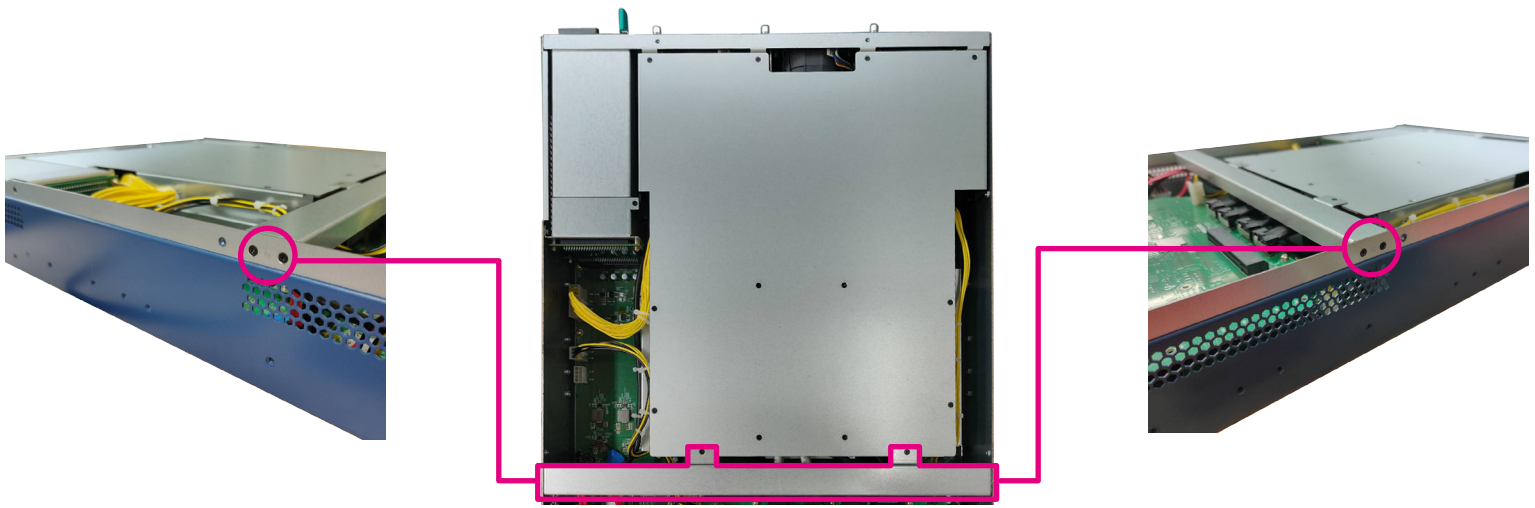
2. With the screws removed, gently slide the cover outwards and then lift up the cover to remove it.

Installing a CPU

The CPU sockets are covered by 3 covers consisting of the front cover, rear cover, and middle cover. To access the CPU sockets, the 3 covers need to be removed first. The following instructions explain how to remove the 3 covers.

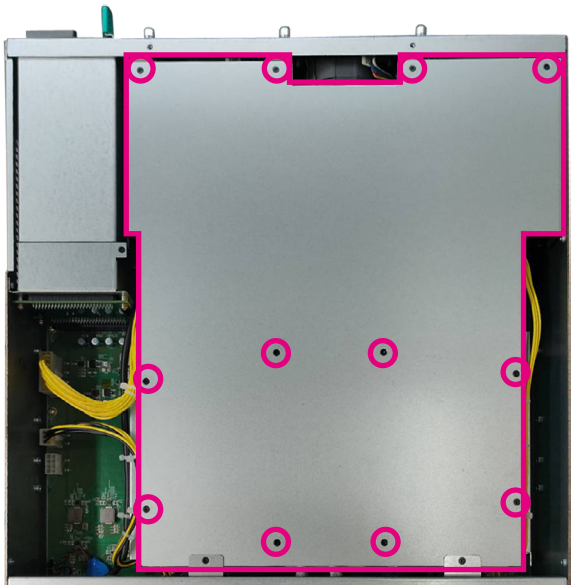
Before installing or removing internal components on the mainboard, please ensure that the AC power cord is unplugged for at least over 20 seconds.

1. With the chassis cover removed, locate the front cover and remove the screws on the top, left, and right side of the front cover.



2. Front cover removed.

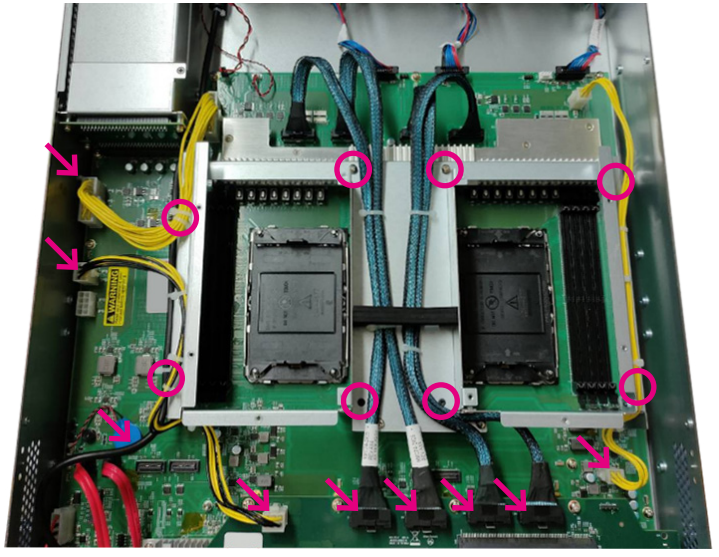
3. Locate the rear cover and remove the screws that secure it, as shown below.



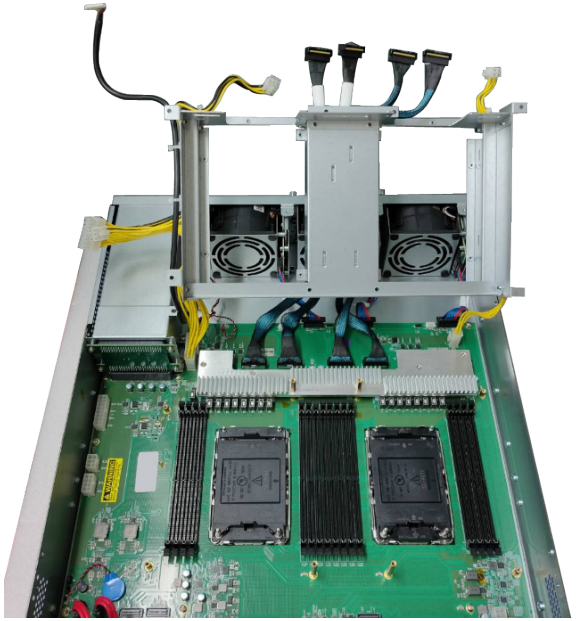
Rear Cover

4. The rear cover is removed.

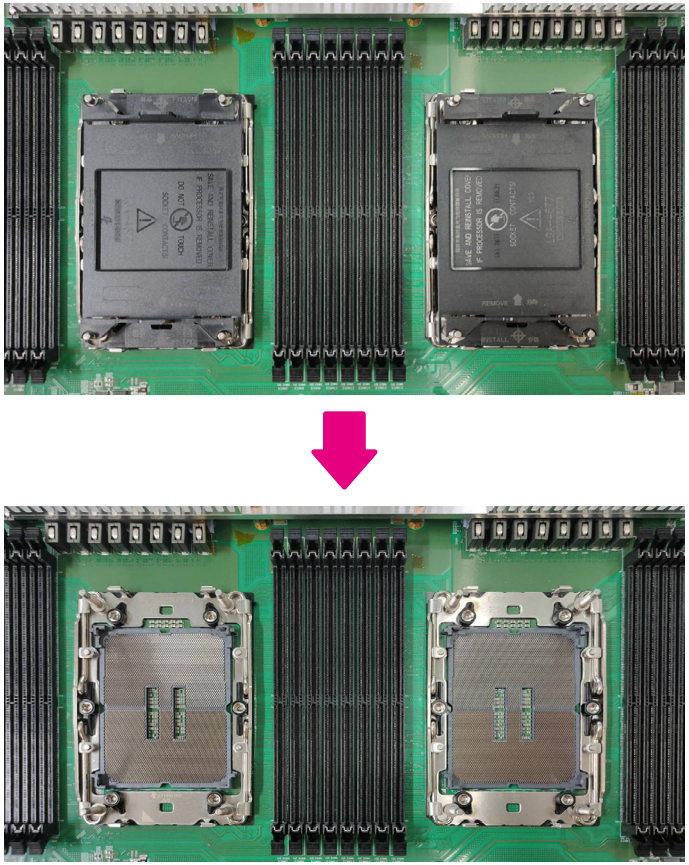
5. Disconnect the cables indicated by arrows and loosen the screws identified by circles.



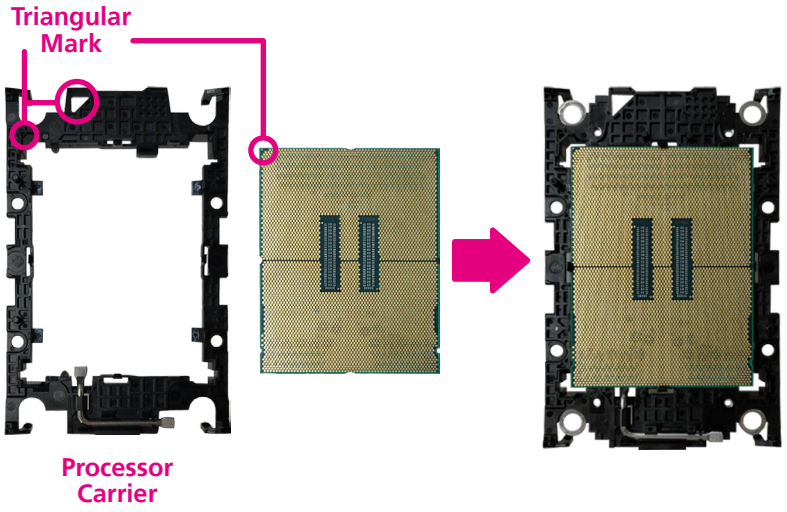
6. Remove the middle cover to fully expose the CPU sockets.



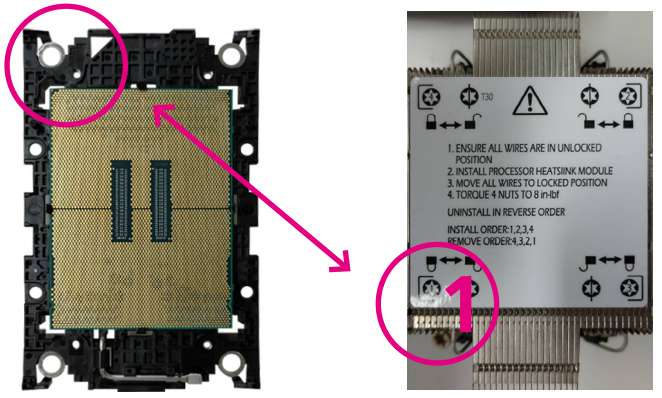
7. Remove the protective cap(s) on the CPU socket(s).

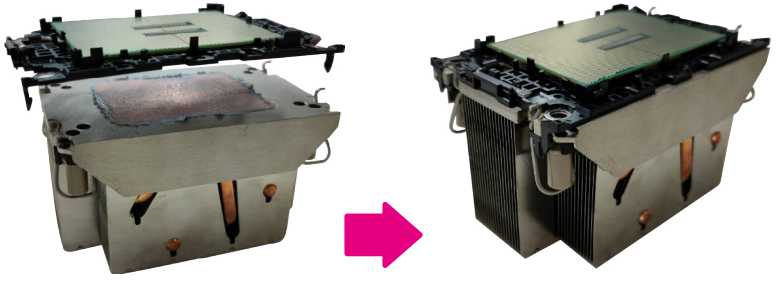


8. Place the CPU into the processor carrier. The triangular mark on the CPU should be aligned with the triangular mark on the processor carrier.

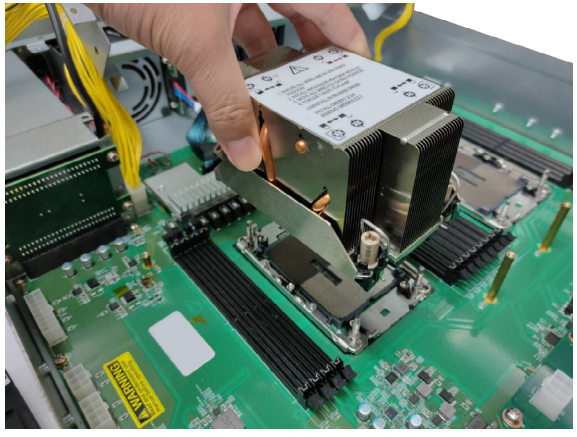


9. Install the processor carrier with the CPU assembled onto the heatsink. Make sure that the triangular mark on the processor carrier aligns with the number 1 marking on the label located at the top of the heatsink, and apply thermal paste.

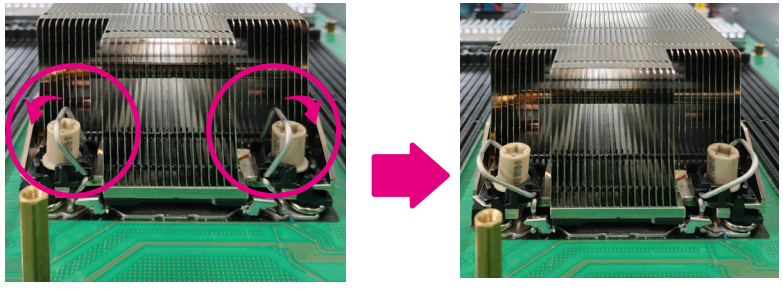




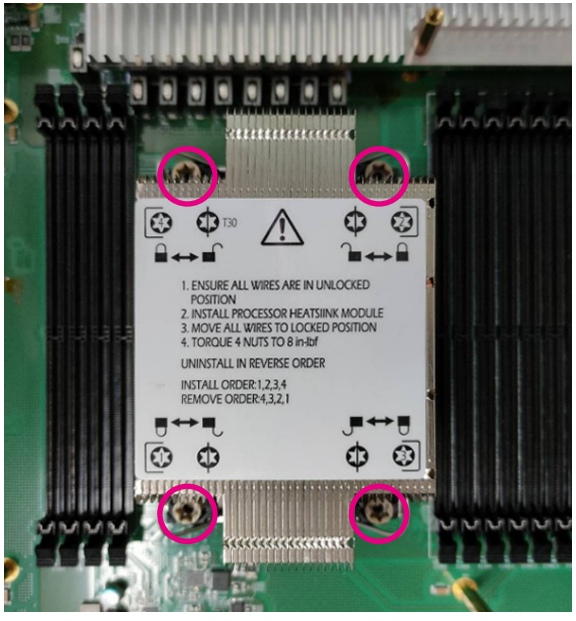
10. Align the heatsink (with the CPU assembled) with the CPU socket, ensuring that the triangular edge of the carrier aligns with the triangular marker on the CPU socket, and then place the heatsink on top of the CPU socket.

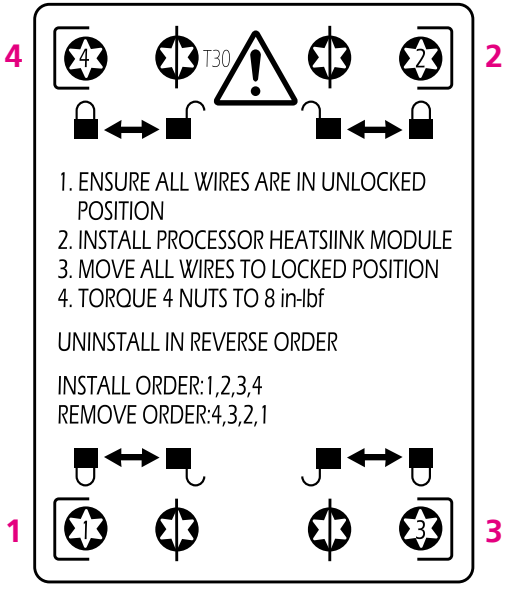


11. Press down on the retention clips to securely attach the heatsink assembly to the CPU socket.



12. Secure the four screws in the order shown on the top of the heatsink or refer to the following images using a T30 screwdriver. Ensure that the screws are tightened with a torque of 6-12 IN-LB.





Please ensure that the T30 screws are tightened with a torque of 6-12 IN-LB. Otherwise, the motherboard may be damaged.

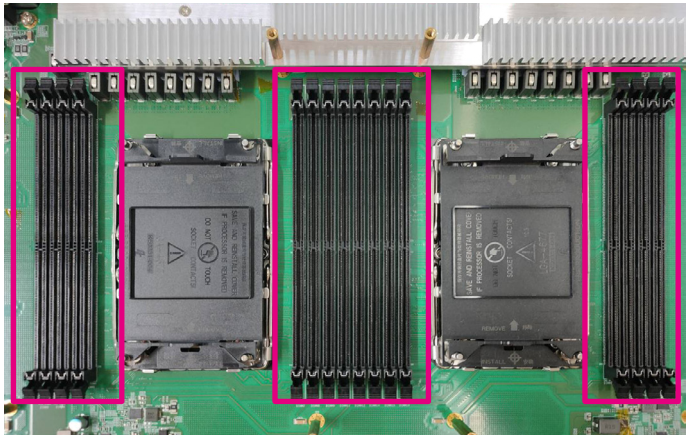
To uninstall the heatsink, remove the screws in reverse order (4 - 3 - 2 - 1) and then release the retention clips by moving them into the unlatch positions.

Installing Memory Modules

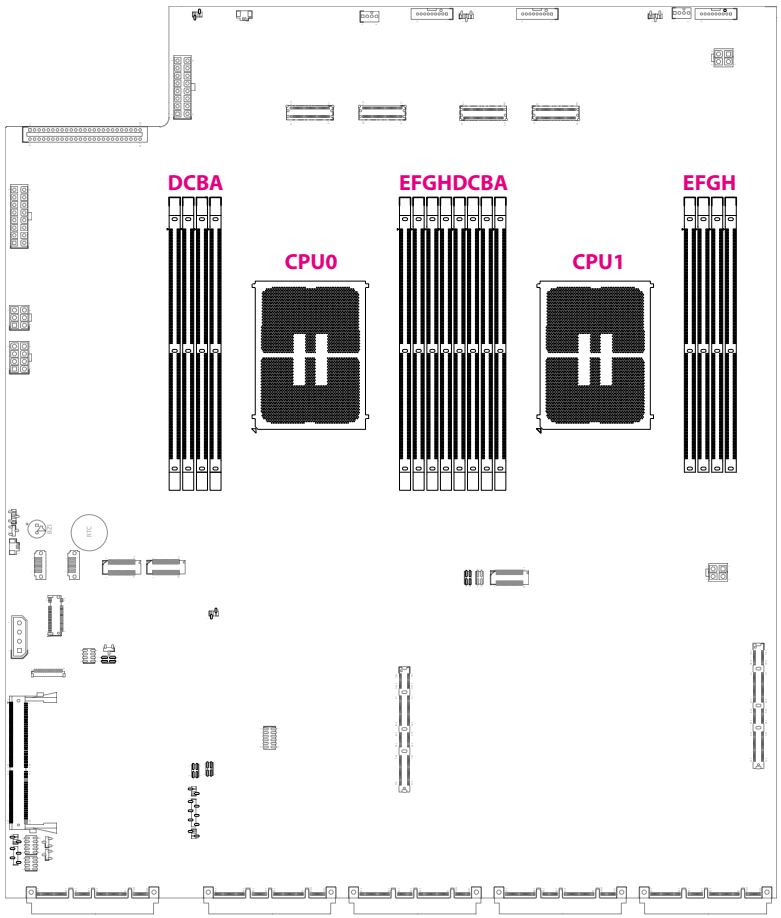
Before beginning the memory installation, please pay attention to the following notices.

- Before installing or removing internal components on the motherboard, please ensure that the AC power cord is unplugged for at least over 20 seconds.
- The memory modules are foolproof design and can only be installed in one direction. If you encounter difficulty, try reversing the module's orientation and avoid using force to prevent damage.
- It is recommended to install memory modules with the same brand, speed, and capacity.
- This motherboard supports up to 1024GB RDIMM DDR5 ECC memory with speeds up to 4800MT/s (1DPC) in 16 DIMM slots.

1. Locate the DIMM sockets on the motherboard and release the locks. Refer to next page for more detailed layout of the CPU sockets and memory slots.



CPU and Memory Layout

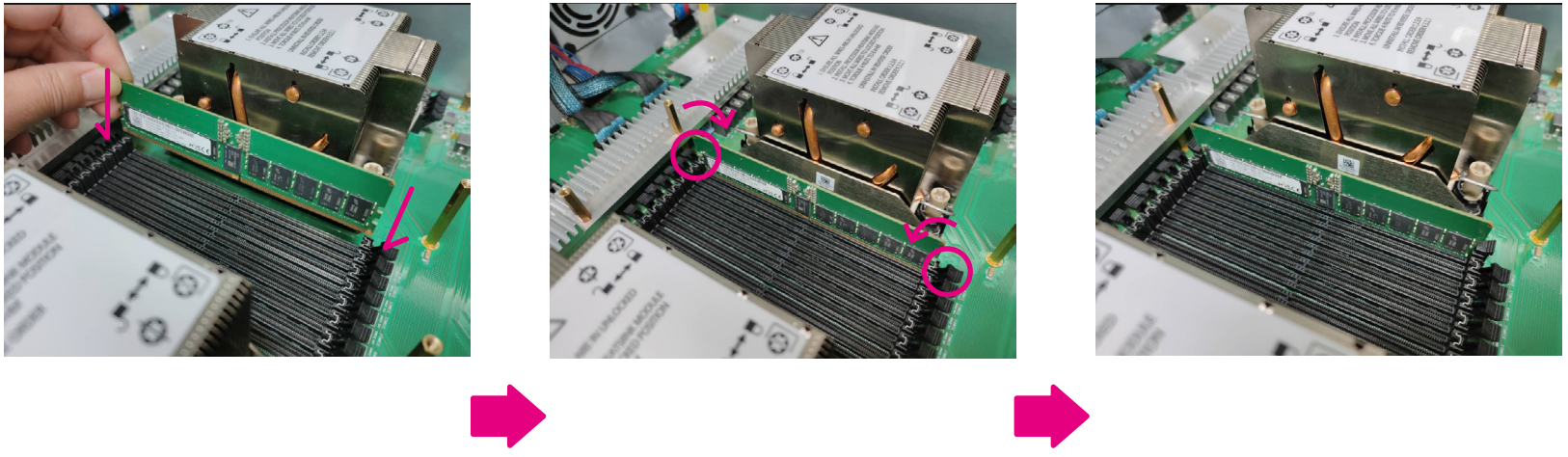


CPU and Memory Module Population Matrix Table

- Refer to the table below for the installation of DDR5 memory DIMM module(s). Ensure that at least one DDR5 DIMM is installed. It is recommended to use RAM modules of the same brand, speed, size, and frequency if multiple RAM modules are required.
- If there is a requirement for a single DIMM installation on the motherboard, please insert the memory module into the DIMM slots of CPU0.

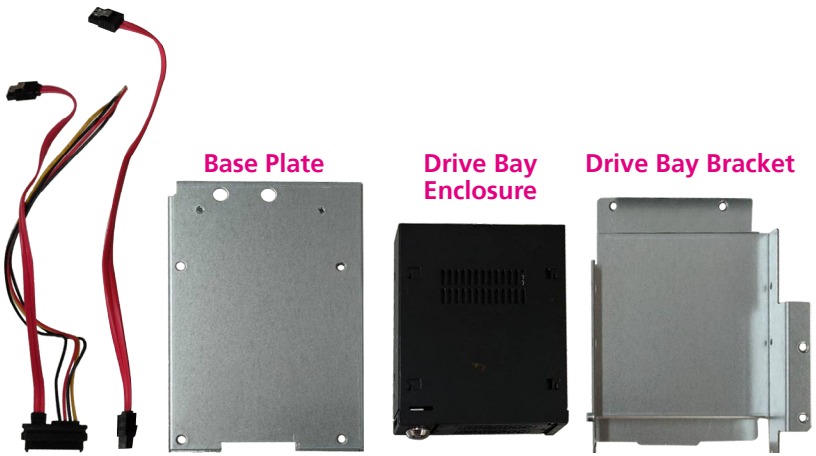
	D	C	B	A	CPU0	E	F	G	H	D	C	B	A	CPU1	E	F	G	H
2 DIMMs				✓									✓					
2 DIMMs						✓									✓			
2 DIMMs			✓									✓						
2 DIMMs							✓									✓		
4 DIMMs				✓				✓					✓				✓	
4 DIMMs		✓				✓					✓				✓			
8 DIMMs		✓		✓		✓		✓			✓		✓		✓		✓	
12 DIMMs	✓	✓		✓		✓	✓	✓		✓	✓		✓		✓	✓	✓	
12 DIMMs		✓	✓	✓		✓		✓	✓		✓	✓	✓		✓		✓	✓
12 DIMMs	✓	✓	✓			✓	✓		✓	✓	✓	✓			✓	✓		✓
12 DIMMs	✓		✓	✓			✓	✓	✓	✓		✓	✓			✓	✓	✓
16 DIMMs	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓

2. Install the memory modules according to the sequence indicated in the memory population table on the previous page.
3. Gently push the locks outward on both ends of the memory slot.
4. Insert the module into the socket at an 90 degree angle. Apply firm even pressure to each end of the module until it slips into the slot. While pushing the module into position, the locks will close automatically.



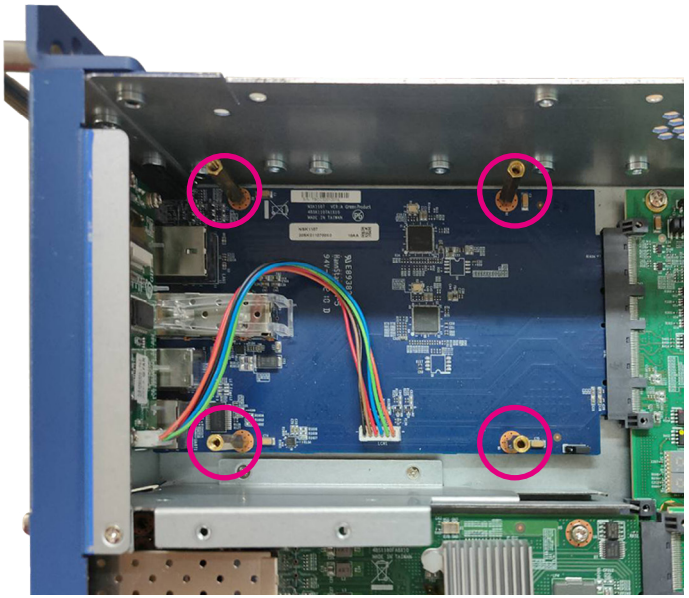
Assembling the 2.5” Removable Drive Bay

The 2.5” removable drive bay kit contains the parts pictured below:

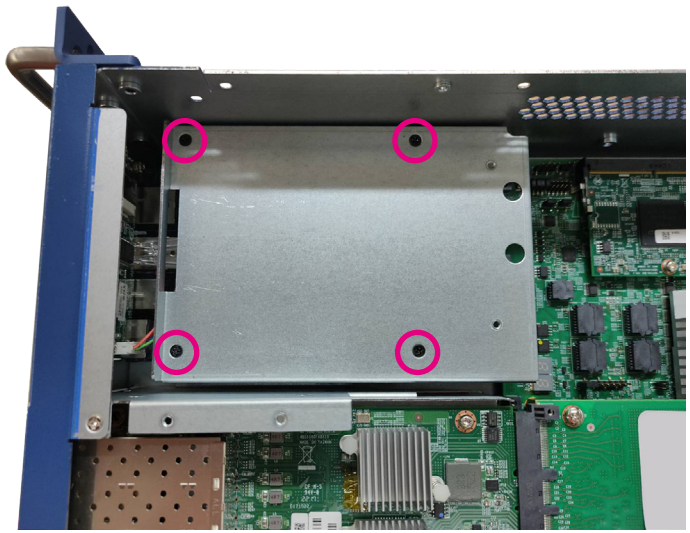


1. With the chassis cover removed, locate the top cover and unscrew the screws on the left and right sides.

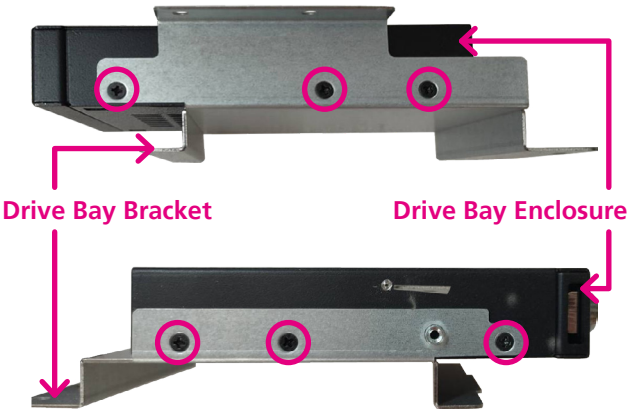
2. Locate the installation position for the drive bay kit and assemble four copper standoffs to the circled locations.



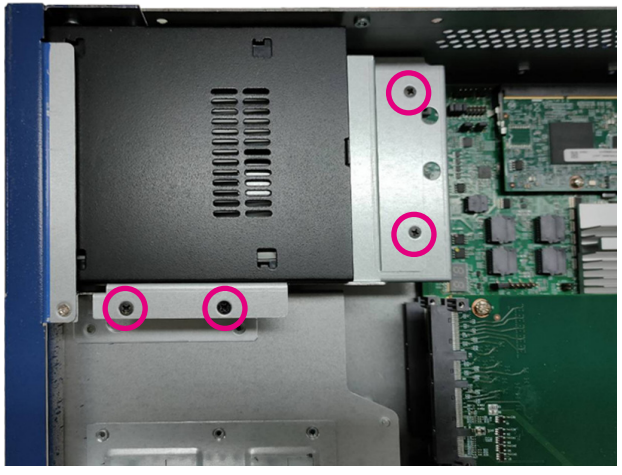
3. Align the mounting holes on the base plate with the copper standoffs, and then secure the base plate to the standoffs using screws.



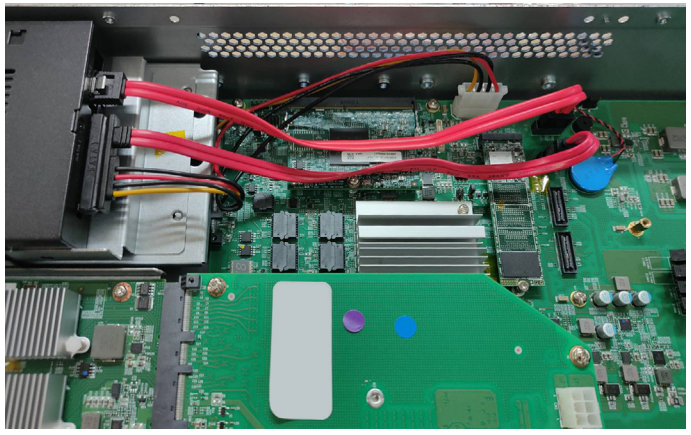
4. Align the mounting holes on the drive bay enclosure with the corresponding mounting holes on the drive bay bracket, and then securely fasten the drive bay enclosure to the bracket using screws.



5. Fix the drive bay bracket to the base plate with screws.



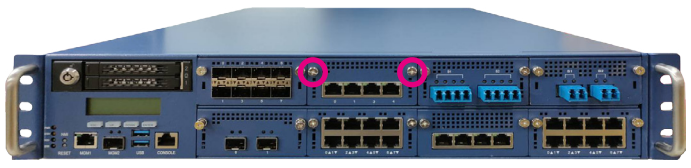
6. Connect the SATA data and power cables to the respective connectors on the motherboard (SATA Connector and SATA Power Connector) and the other ends of the cables to the connectors on the drive bay enclosure.



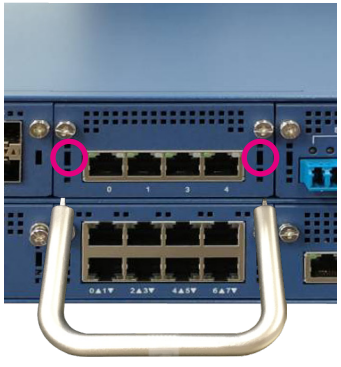
Installing the LAN Module

Please correctly follow the below instructions and noted items to avoid making unnecessary damages. Make sure the power supply is switched off and disconnected from the power sources before replacing or adding LAN modules to prevent electric shock or system damage.

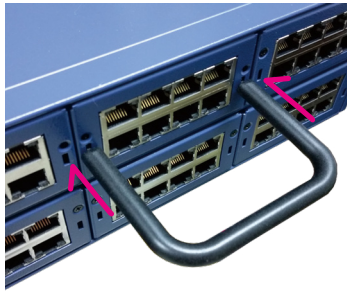
1. Find the slot where you want to install the LAN module and loosen the screws on both sides.



2. Use the handle provided, and insert the handle into the two holes on the LAN module.

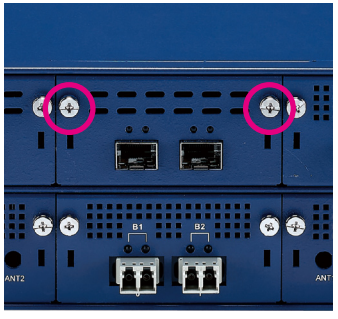


Handle



3. Once the handle is firmly secured in position, pull the handle outwards to remove the LAN module.

4. Insert the desired module into the slot and secure the module with the two screws.



Important:
Before using Optical fiber for transferring data, make sure you have connected an approved Optical Transceiver Module. User needs to install appropriate and UL approved Laser Class I Transceivers, rated 3.3Vdc, max. 1W.

Plugging the Internal Power Connector

The system provides external power connectors for expansion cards such as riser boards or FHFL cards. Please note that these power connectors have positive and negative terminals. To prevent damage to the motherboard, do not forcefully plug the power connectors in the wrong direction, even though they have a fool-proof design. Refer to Chapter 2 for pin definitions of the power connectors.

Chapter 4: BIOS Setup

This chapter describes how to use the BIOS setup program for NSA 7160. The BIOS screens provided in this chapter are for reference only and may change if the BIOS is updated in the future.

To check for the latest updates and revisions, visit the NEXCOM website at www.nexcom.com.tw.

About BIOS Setup

The BIOS (Basic Input and Output System) Setup program is a menu driven utility that enables you to make changes to the system configuration and tailor your system to suit your individual work needs. It is a ROM-based configuration utility that displays the system's configuration status and provides you with a tool to set system parameters.

These parameters are stored in non-volatile battery-backed-up CMOS RAM that saves this information even when the power is turned off. When the system is turned back on, the system is configured with the values found in CMOS.

With easy-to-use pull down menus, you can configure such items as:

- Hard drives, diskette drives, and peripherals
- Video display type and display options
- Password protection from unauthorized use
- Power management features

The settings made in the setup program affect how the computer performs. It is important, therefore, first to try to understand all the setup options, and second, to make settings appropriate for the way you use the computer.

When to Configure the BIOS

- This program should be executed under the following conditions:
- When changing the system configuration
- When a configuration error is detected by the system and you are prompted to make changes to the setup program
- When resetting the system clock
- When redefining the communication ports to prevent any conflicts
- When making changes to the Power Management configuration
- When changing the password or making other changes to the security setup

Normally, CMOS setup is needed when the system hardware is not consistent with the information contained in the CMOS RAM, whenever the CMOS RAM has lost power, or the system features need to be changed.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering Setup

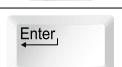
When the system is powered on, the BIOS will enter the Power-On Self Test (POST) routines. These routines perform various diagnostic checks; if an error is encountered, the error will be reported in one of two different ways:

- If the error occurs before the display device is initialized, a series of beeps will be transmitted.
- If the error occurs after the display device is initialized, the screen will display the error message.

Powering on the computer and immediately pressing 

allows you to enter Setup.

Legends

Key	Function
	Moves the highlight left or right to select a menu.
	Moves the highlight up or down between sub-menu or fields.
	Exits the BIOS Setup Utility.
	Scrolls forward through the values or options of the highlighted field.
	Scrolls backward through the values or options of the highlighted field.
	Selects a field.
	Displays General Help.
	Load previous values.
	Load optimized default values.
	Saves and exits the Setup program.
	Press <Enter> to enter the highlighted sub-menu

Scroll Bar

When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu

When "▶" appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press 

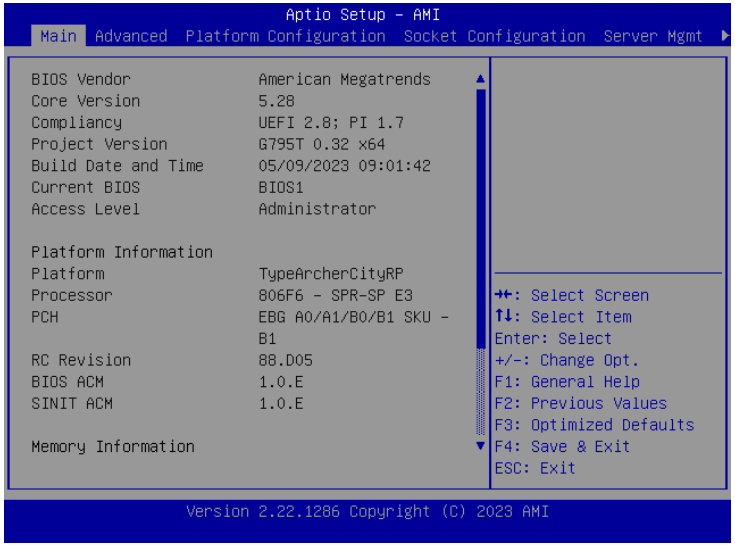
.

BIOS Setup Utility

Once you enter the AMI BIOS Setup Utility, the Main Menu will appear on the screen. The main menu allows you to select from several setup functions and one exit. Use arrow keys to select among the items and press Enter to accept or enter the submenu.

Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <day>, <month>, <date>, <year>. Day displays a day, from Monday to Sunday. Month displays the month, from January to December. Date displays the date, from 1 to 31. Year displays the year, from 1998 to 9999.

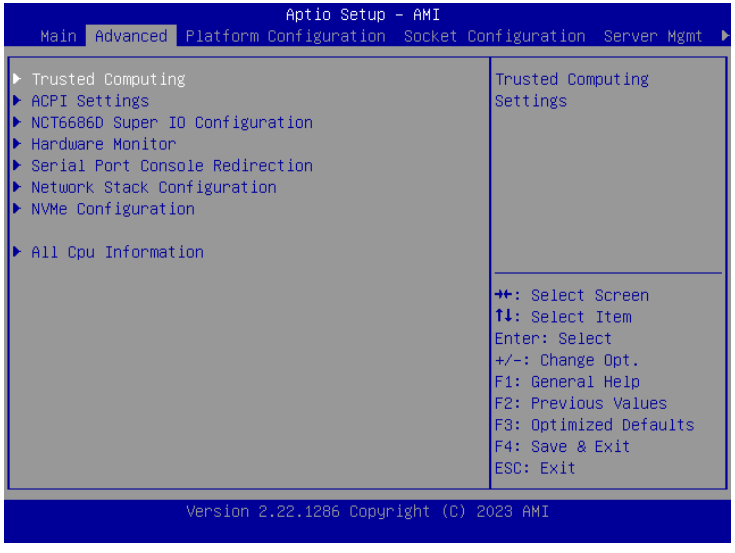
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

Advanced

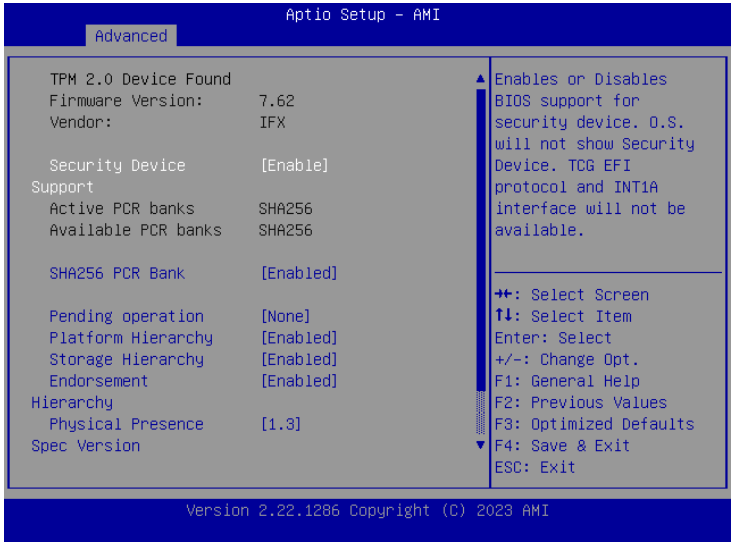
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Setting incorrect field values may cause the system to malfunction.



Advanced > Trusted Computing

This section is used to configure Trusted Platform Module (TPM) settings.



Security Device Support
Enables or disables BIOS support for security device. O.S will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

SHA-1 PCR Bank
Enables or disables SHA-1 PCR Bank.

SHA256 PCR Bank
Enables or disables SHA256 PCR Bank.

Pending operation
Schedules an operation for the security device.

Platform Hierarchy
Enables or disables platform hierarchy.

Storage Hierarchy
Enables or disables storage hierarchy.

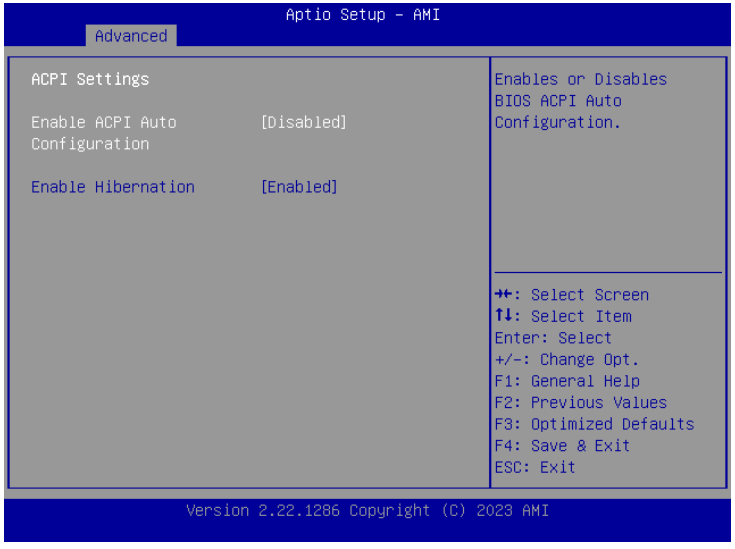
Endorsement Hierarchy
Enables or disables endorsement hierarchy.

Physical Presence Spec Version
Configures the physical presence spec version.

Device Select
TPM 1.2 will restrict support to TPM 1.2 devices. TPM 2.0 will restrict support to TPM 2.0 devices. Auto will support both TPM 1.2 and 2.0 devices with the default set to TPM 2.0 devices if not found, and TPM 1.2 devices will be enumerated.

Advanced > ACPI Settings

This section is used to configure the serial port.

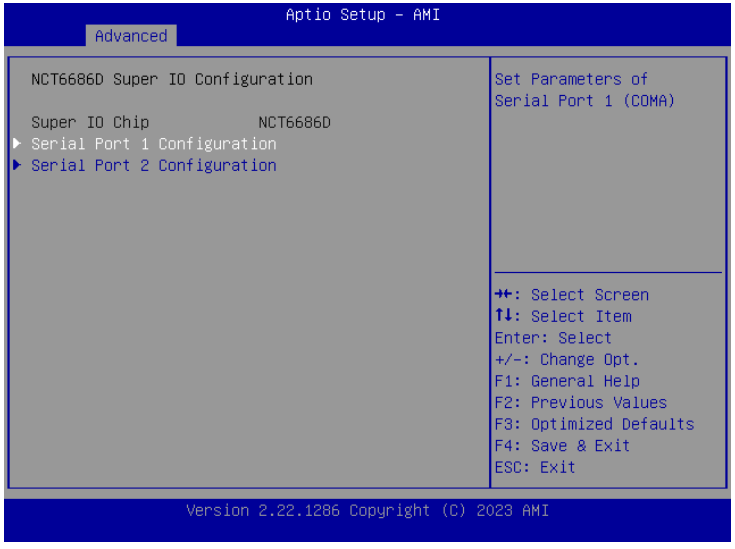


Enable ACPI Auto Configuration
Enables or disables AMT BIOS features. When disabled, user will no longer be able to access MEBx setup.

Enable Hibernation
Enables or disables system ability to hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems

Advanced > NCT6686D Super IO Configuration

This section is used to configure the serial port.



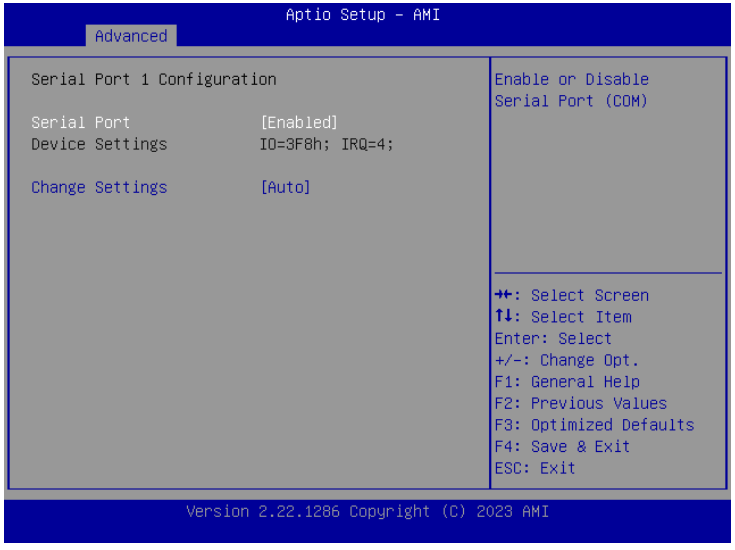
Super IO Chip
Displays the Super I/O chip used on the board.

Serial Port 1 Configuration
Configuration settings for serial port 1.

Serial Port 2 Configuration
Configuration settings for serial port 2.

Advanced > NCT6686D Super IO Configuration > Serial Port 1 Configuration

This section is used to configure serial port 1.

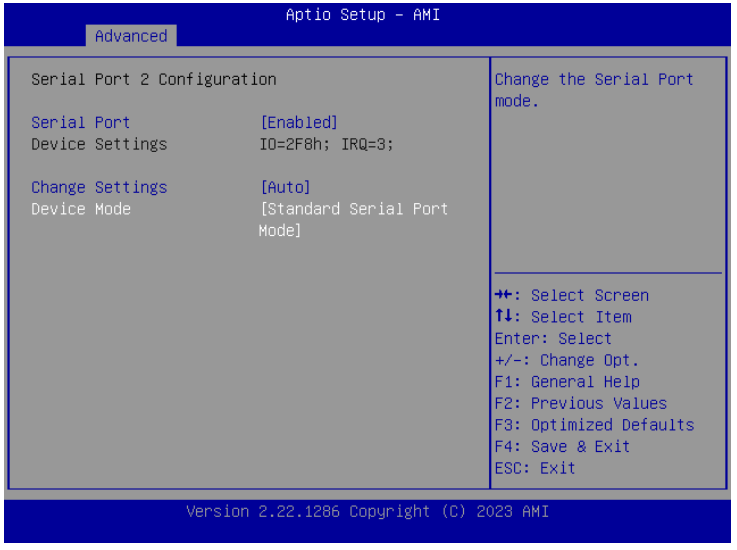


Serial Port
Enables or disables the serial port.

Change Settings
Selects an optimal setting for the Super IO device.

Advanced > NCT6686D Super IO Configuration > Serial Port 2 Configuration

This section is used to configure serial port 2.



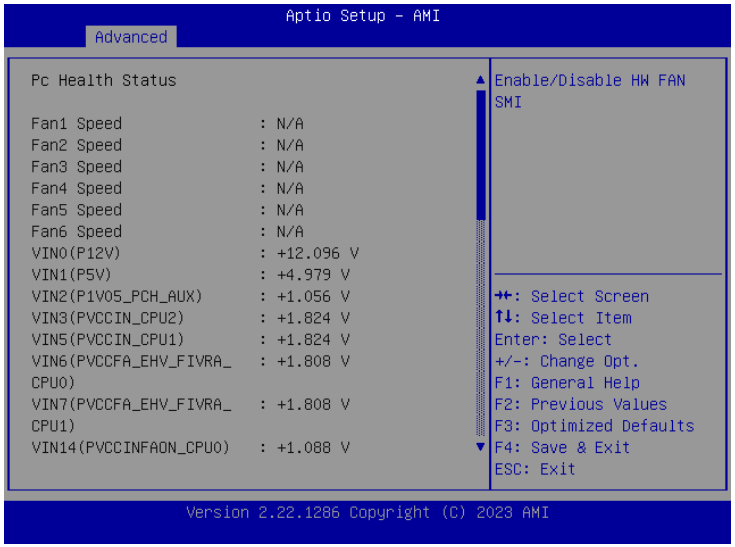
Serial Port
Enables or disables the serial port.

Change Settings
Selects an optimal setting for the Super IO device.

Device Mode
Configures the operating mode of the serial port

Advanced > Hardware Monitor

This section is used to monitor hardware status such as temperature, fan speed and voltages.



Fan1/2/3/4/5/6 Speed
Detects and displays the fan speeds.

VIN0(P12V)/
VIN1(P5V)/
VIN2(P1V05_PCH_AUX)/
VIN3(PVCCIN_CPU2)/
VIN5(PVCCIN_CPU1)/
VIN6(PVCCFA_EHV_FIVRA_CPU0)/
VIN7(PVCCFA_EHV_FIVRA_CPU1)/
VIN14(PVCCINFAON_CPU0)/
VIN16(PVNN_PCH_AUX)/
VCC3V/
VBAT
Detects and displays the output voltages.

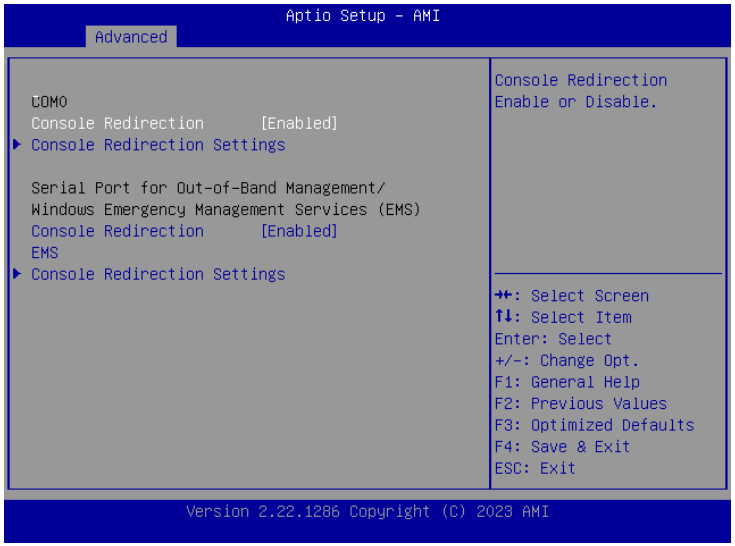
HW FAN SMI
Enables or disables the HW FAN SMI.

FAN SMI1/2/3/4/5/6
Enables or disables the FAN SMI1/2/3/4/5/6.

HW Voltage SMI
VIN0(P12V) SMI/
VIN1(P5V) SMI/
VIN2(P1V05_PCH_AUX) SMI/
VIN3(PVCCIN_CPU2) SMI/
VIN5(PVCCIN_CPU1) SMI/
VIN6(PVCCFA_EHV_FIVRA_CPU0) SMI/
VIN7(PVCCFA_EHV_FIVRA_CPU1) SMI/
VIN14(VIN14(PVCCINFAON_CPU0) SMI/
VIN15(VIN14(PVCCINFAON_CPU1) SMI/
VIN16(PVNN_PCH_AUX) SMI/
VCC3V SMI/
VBAT SMI
Enables or disables the HW Voltage SMI.

Advanced > Serial Port Console Redirection

This section is used to configure the serial port that will be used for console redirection.

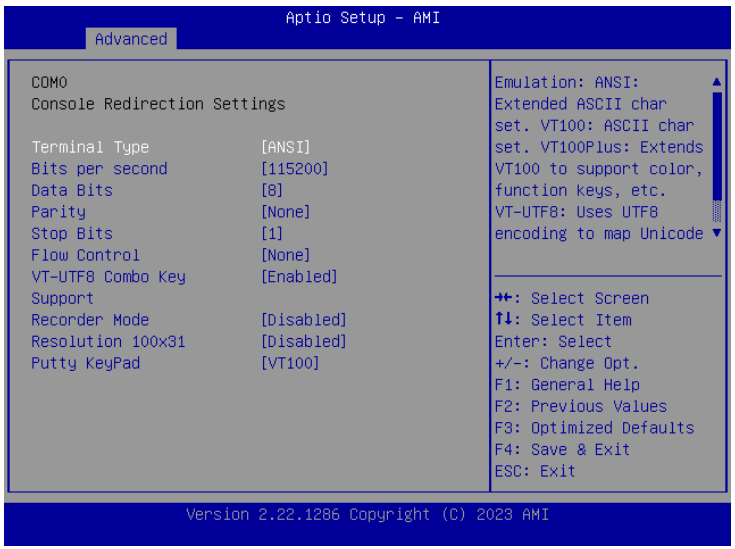


Console Redirection

Enables or disables console redirection for COM0.

Advanced > Serial Port Console Redirection > Console Redirection Settings

Specifies how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.



Terminal Type

ANSI	Extended ASCII character set.
VT100	ASCII character set.
VT100+	Extends VT100 to support color, function keys, etc.
VT-UTF8	Uses UTF8 encoding to map Unicode characters onto 1 or more bytes.

Bits Per Second

Selects the serial port transmission speed. The speed must match the other side. Long or noisy lines may require a lower speed.

Data Bits

The options are 7 and 8.

Parity

A parity bit can be sent with the data bits to detect some transmission errors.

Even	Parity bit is 0 if the number of 1's in the data bits is even.
Odd	Parity bit is 0 if number of 1's in the data bits is odd.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Flow Control

Flow control can prevent data loss from buffer overflow. When sending data and the receiving buffers are full, a "stop" signal can be sent to stop the data flow.

VT-UTF8 Combo Key Support

Enables or disables VT-UTF8 combo key support.

Recorder Mode

When this field is enabled, only text will be sent. This is to capture the terminal data.

Resolution 100x31

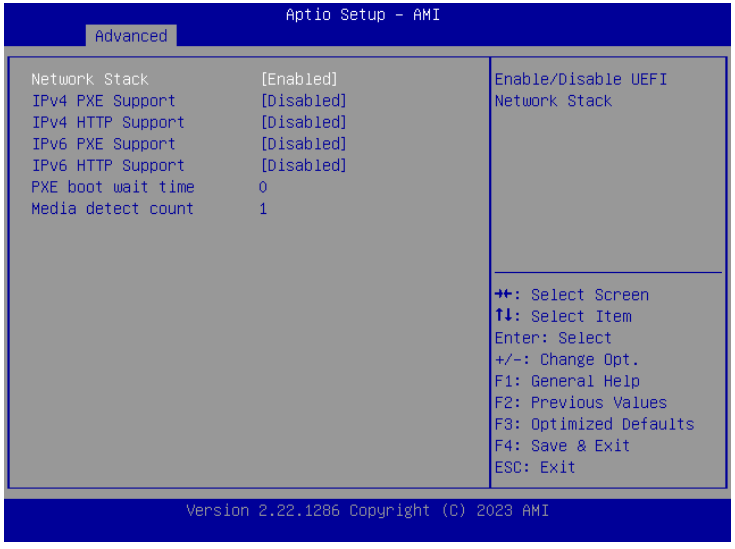
Enables or disables extended terminal resolution.

Putty KeyPad

Selects the Putty keyboard emulation type.

Advanced > Network Stack Configuration

This section is used to configure the network stack.



Network Stack
Enables or disables UEFI network stack. More options will appear when selecting Enabled. If Enabled is selected, more options will appear on the screen.

IPv4 PXE Support
Enables or disables IPv4 PXE support. If disabled, the IPv4 boot option will not be created.

IPv4 HTTP Support
Enables or disables IPv4 HTTP support.

IPv6 PXE Support
Enables or disables IPv6 PXE support. If disabled, the IPv6 boot option will not be created.

IPv6 HTTP Support
Enables or disables IPv6 HTTP support.

PXE boot wait time
Configures the wait time to press the ESC key to abort the PXE boot.

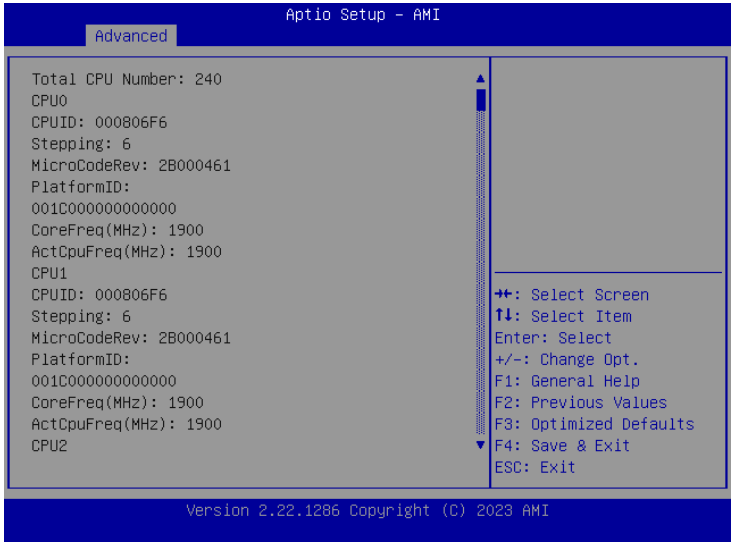
Media detect count
Configures the number of times the media will be checked.

Advanced > NVMe Configuration

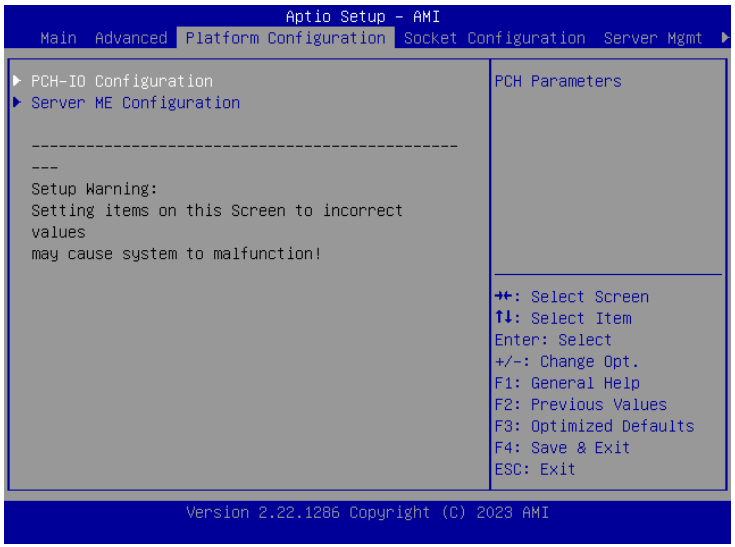
This section is used to display information on the NVMe devices installed.

Advanced > All Cpu Information

This section is used to display information on the installed CPUs.



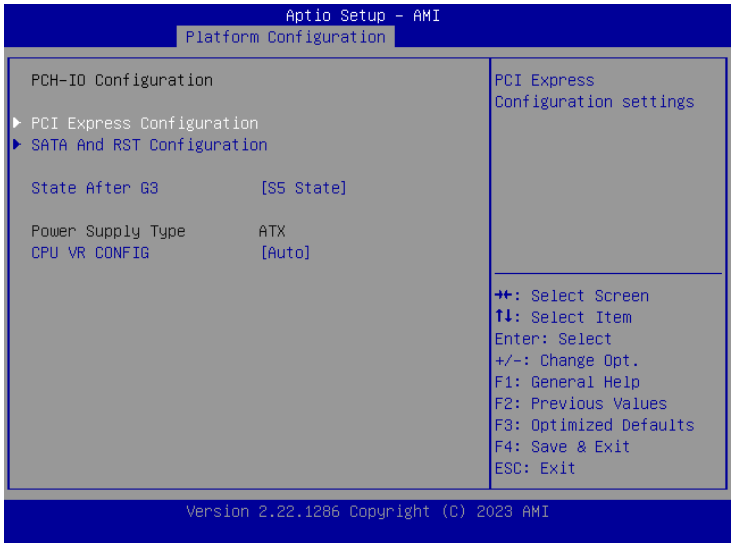
Platform Configuration



PCH-IO Configuration
Enters the PCH Configuration submenu.

Server ME Configuration
Enters the Server ME Configuration submenu.

Platform Configuration > PCH-IO Configuration



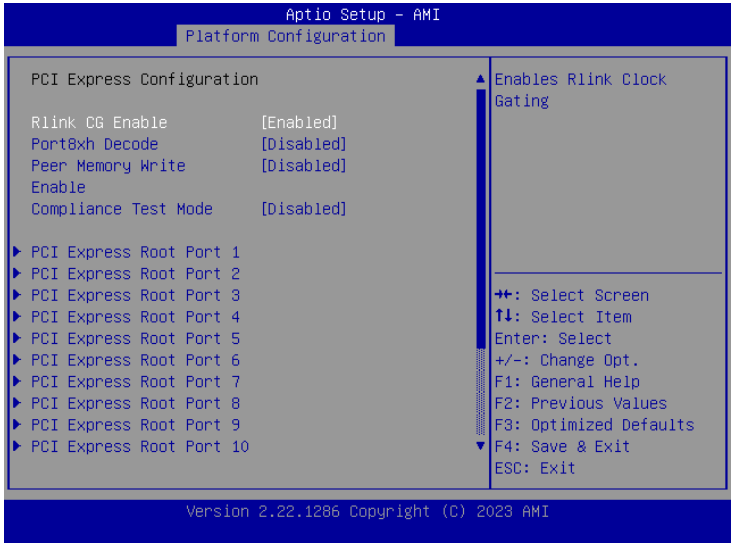
PCI Express Configuration
Enters the PCI Express Configuration submenu.

SATA and RST Configuration
Enters the SATA and RST Configuration submenu.

SATA After G3
Enters the SATA After G3 submenu.

CPU VR CONFIG
Enables or disables CPU VR Config.

Platform Configuration > PCH-IO Configuration > PCI Express Configuration



Rlink CG Enable
Enables or disables the rlink clock gating.

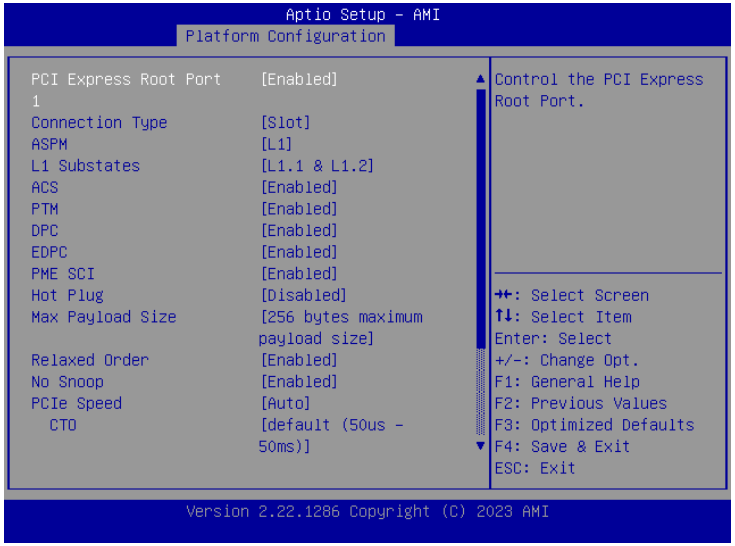
Port8xh Decode
Enables or disables the Port8xh Decode.

Peer Memory Write Enable
Enables or disables the Peer Memory Write.

Compliance Test Mode
Enables or disables the Compliance Test Mode.

PCI Express Root Port 1~n
Enters the PCI Express Root Port submenu.

Platform Configuration > PCH-IO Configuration > PCI Express Configuration > PCI Express Root Port 1 to 10



PCI Express Root Port 1 ~ 10
Enables or disables the PCI Express port.

Connection Type
Selects a connection type.

ASPM Support
Selects the ASPM level.

L1 Substates
Configures the L1 Substates settings.

ACS
Enables or disables the ACS.

PTM
Enables or disables the PTM.

DCP
Enables or disables the DCP.

EDPC
Enables or disables the EDPC.

PME SCI
Enables or disables the PME SCI.

Hot Plug
Enables or disables the hot plug.

Max Payload Size
Configures the PCIe maximum payload size.

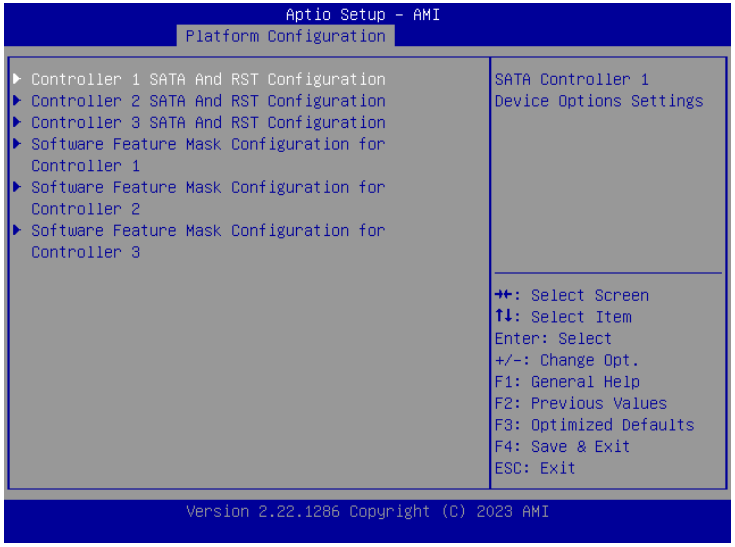
Relaxed Order
Enables or disables the PCI Express device's relaxed order.

No Snoop
Enables or disables the no snoop.

PCIe Speed
Configures the speed of the PCI Express port.

CT0
Configures the CT0 for PCI Express.

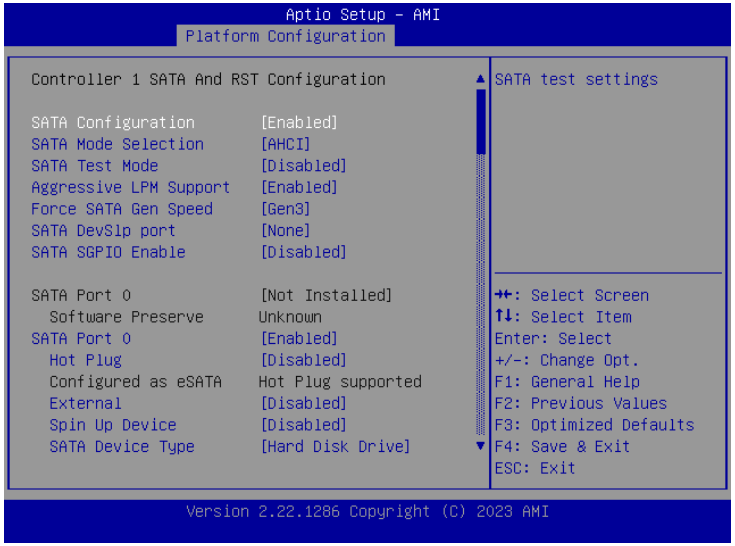
Platform Configuration > PCH-IO Configuration > SATA and RTS Configuration



Controller 1/2/3 SATA and RST Configuration
Enters the Controller SATA and RST Configuration submenu.

Software Feature Mask Configuration for Controller 1/2/3
Enters the Software Feature Mask Configuration for Controller submenu.

Platform Configuration > PCH-IO Configuration > SATA and RTS Configuration > Controller 1 / 2 / 3 SATA And RST Configuration



SATA Configuration
Enables or disables the SATA configuration.

SATA Mode Selection
Configures the SATA mode.

SATA Test Mode
Enables or disables the SATA test mode.

Aggressive LPM Support
Enables or disables the aggressive LPM support.

Force SATA Gen Speed
Forces to select the SATA speed.

SATA DevSlp port
Configures the SATA DevSlp port.

SATA SGPIO Enable
Enables or disables the **SATA SGPIO**.

SATA Port 0
Enables or disables the SATA Port 0.

Hot Plug
Enables or disables hot plugging feature on SATA port 0.

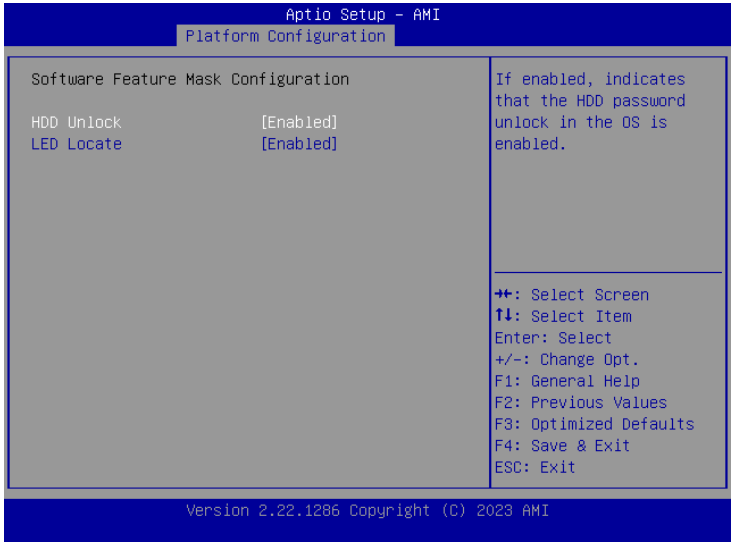
External
Enables or disables the feature of External.

Spin Up Device
Enables or disables staggered spin up on devices connected to SATA port 1.

SATA Device Type
Identifies what type of SATA device is connected.

DIT0 Configuration
Enables or disables DIT0 configuration for SATA Port.

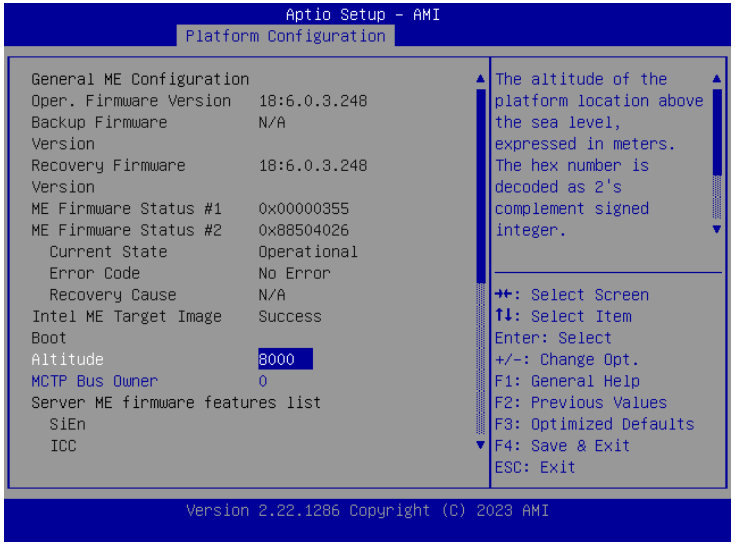
Platform Configuration > PCH-IO Configuration > SATA and RTS Configuration > Software Feature Mask Configuration for controller 1 / 2 / 3



HDD Unlock
Enables or disables HDD password unlock in the OS.

LED Locate
Enables or disables detection of LED/SGPIO hardware and ping-to-locate feature.

Platform Configuration > Server ME Configuration



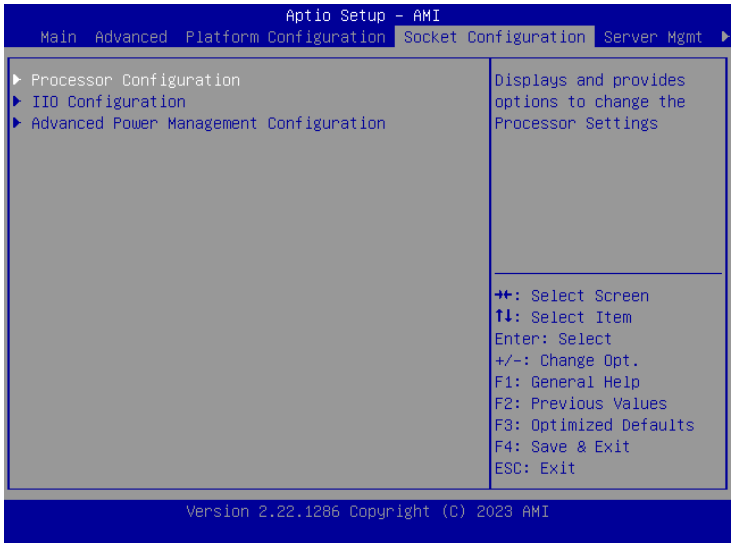
Attitude

The altitude of the platform location above the sea level, expressed in meters. The hex number is decoded as 2's complement signed integer.

MCTP Bus Owner

Configures the MCTP Bus Owner.

Socket Configuration



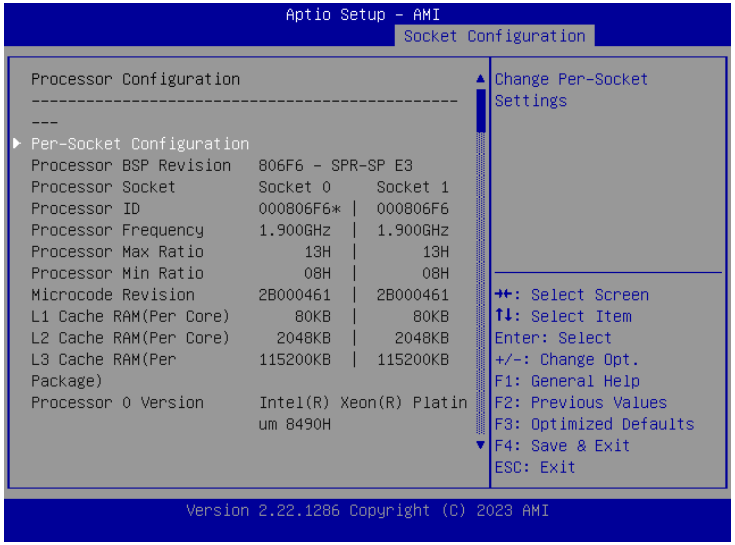
Processor Configuration
Enters the Processor Configuration submenu.

UPI Configuration and Memory Configuration
Enters the UPI Configuration and Memory Configuration submenu.

IIO Configuration
Enters the IIO Configuration submenu.

Advanced Power Management Configuration
Enters the Advanced Power Management Configuration submenu.

Socket Configuration > Processor Configuration



Enable LP [Global]
Configures the option of Enable LP.

Skip Flex Ratio Override
Enables or disables the Skip Flex Ratio Override.

Check CPU BIST Result
Enables or disables the Check CPU BIST Result.

33trikerTimer
Enables or disables the 33trikerTimer.

Fast String
Enables or disables the Fast String.

Machine Check
Enables or disables the Machine Check.

Hardware Prefetcher
Enables or disables the MLC streamer prefetcher.

L2 RFO Prefetch Disable
Enables or disables L2 RFO prefetch.

Adjacent Cache Prefetcher
Enables or disables prefetching of adjacent cache lines.

DCU Streamer Prefetcher
Enables or disables the DCU Streamer Prefetcher.

DCU IP Prefetcher
Enables or disables the DCU IP Prefetcher.

LLC Prefetch
Enables or disables the DLLC Prefetch.

FB Thread Slicing
Enables or disables the FB Thread Slicing.

AMP Prefetch
Enables or disables the AMP Prefetch.

BSP Selection
Configures the option of BSP Selection.

Extended APIC
Enables or disables extended APIC support.

APIC Physical Mode
Enables or disables the APIC Physical Mode.

Legacy Agent
Enables or disables the Legacy Agent.

SMBus Agent
Enables or disables the SMBus Agent.

IE Agent
Enables or disables the IE Agent.

Generic Agent
Enables or disables the Generic Agent.

eSPI Agent
Enables or disables the eSPI Agent.

DfxRedManu Agent
Enables or disables the DfxRedManu Agent.

DfxOragne Agent
Enables or disables the DfxOrange Agent.

DBP-F
Enables or disables the DBP-F.

IIO LLC Ways [14:0] (Hex)
Configures the option of IIO LLC Ways.

SMM Blocked and Delayed
Enables or disables the SMM Blocked and Delayed.

eSMM Save State
Enables or disables the eSMM Save State.

SMBus Error Recovery
Enables or disables the SMBus Error Recovery.

Enable Intel(R) TXT
Enables or disables the Intel® TXT support.

VMX
Enables or disables the Virtual Machine Extensions.

SMBus Error Recovery
Enables or disables the SMBus Error Recovery.

Enable SMX
Enables or disables the Secure Mode Extensions.

Lock Chipset
Locks or unlocks the chipset.

MSR Lock Control
Enables or disables the MSR Lock Control.

PPIN Control
Unlock or enables the PPIN Lock.Lock Chipset
AES-NI
Enables or disables the AES-NI support.

Memory Encryption (TME)
Enables or disables the memory encryption.

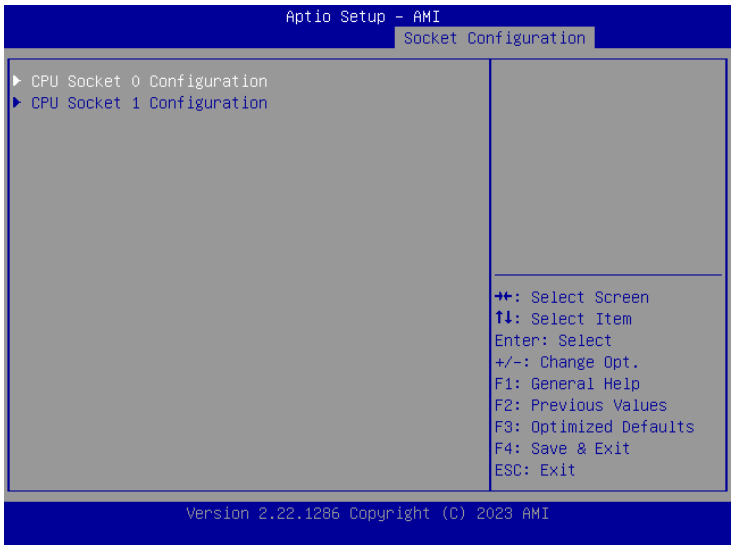
In Field Scan
Enters the In Field Scan submenu.

PSMI Configuration
Enters the PSMI Configuration submenu.

Processor Dfx Configuration
Enters the Processor Dfx Configuration submenu.

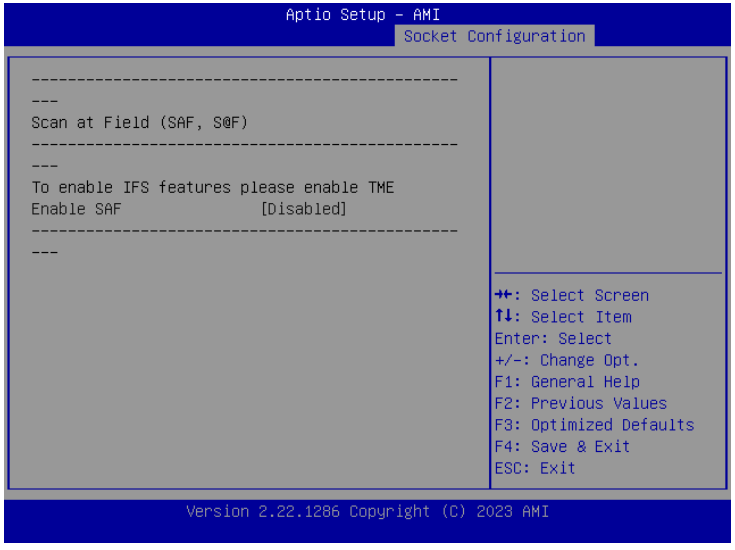
Processor CFR Configuration
Enters the Processor CFR Configuration submenu.

Socket Configuration > Processor Configuration > Per-Socket Configuration



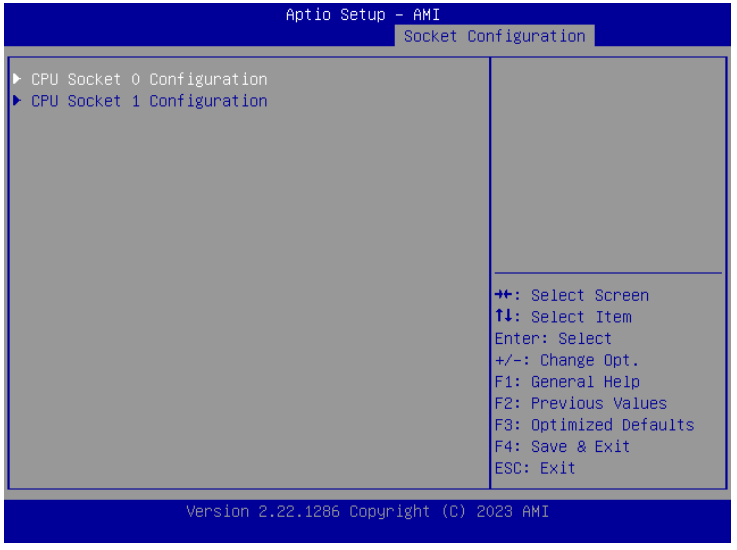
CPU Socket 0/1 Configuration
Enters CPU Socket 0/1 Configuration submenu.

Socket Configuration > Processor Configuration > In Field Scan



Scan at Field
To enable IFS features please enable TME Enable SAF.

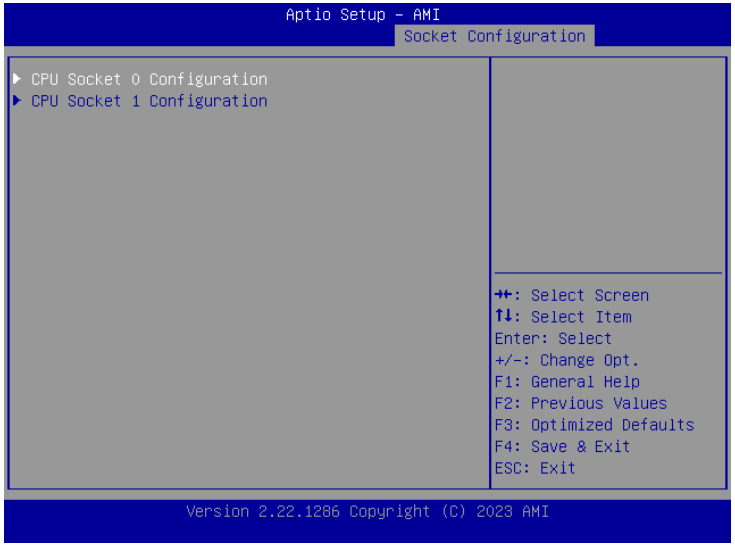
Socket Configuration > Processor Configuration > PSMI Configuration



Global PSMI Enable
Enables or disables the Global PSMI.

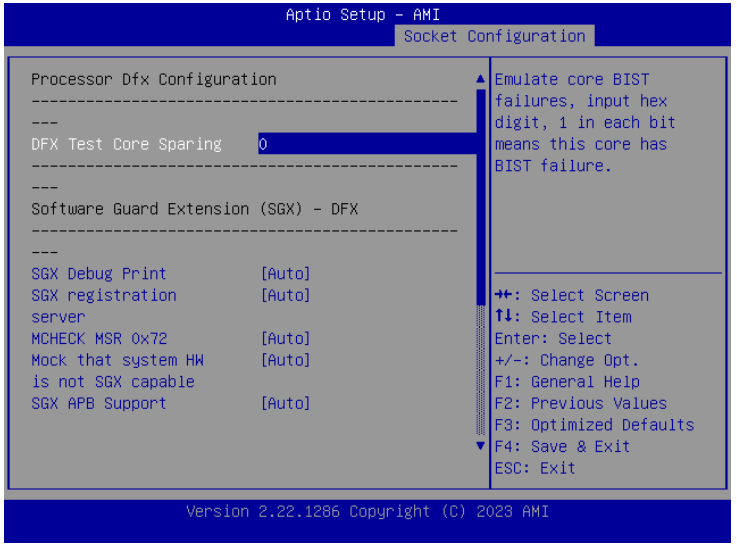
Socket 0/1 Configuration
Enters the Socket 0/1 Configuration submenu.

Socket Configuration > Processor Configuration > PSMI Configuration > Socket 0/1 Configuration



Socket 0/1 Configuration
Enables or disables PSMI.

Socket Configuration > Processor Configuration > Processor Dfx Configuration



DFX Test Core Sparing
Emulate core BIST features, input hex digit, 1 in each bit means this core has BIST failure.

SGX Debug Print
Configures the SGX Debug Print.

SGX registration server
Configures the SGX registration server.

MCHECK MSR 0x72
Configures the MCHECK MSR 0x72.

Mock that system HW is not SGX capable
Configures the Mock that system HW is not SGX capable.

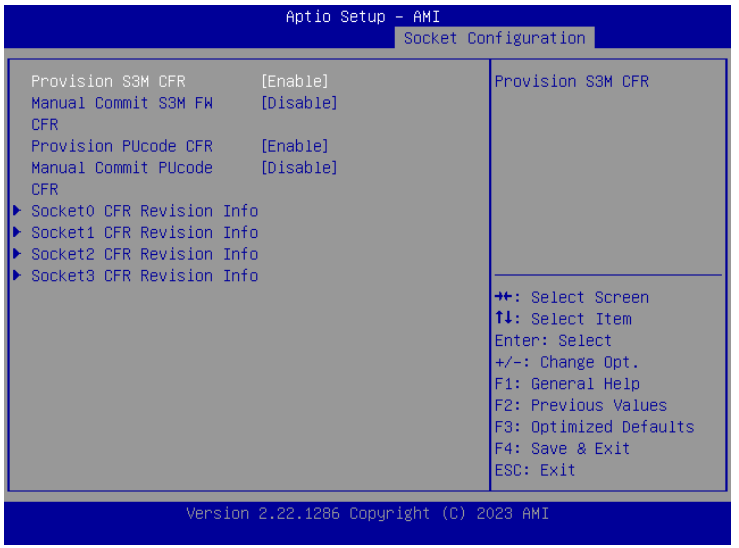
SGX APB Support
Configures the SGX APB Support.

Skip checking promote of warm reset to cold reset
Configures the Skip checking promote of warm reset to cold reset.

Allow SGX with non-POR memory population
Enable or disable the Allow SGX with non-POR memory population.

ACTM Enable
Enable or disable the ACTM Enable.

Socket Configuration > Processor Configuration > Processor CFR Configuration



Provision S3M CFR
Enable or disable the Provision S3M CFR.

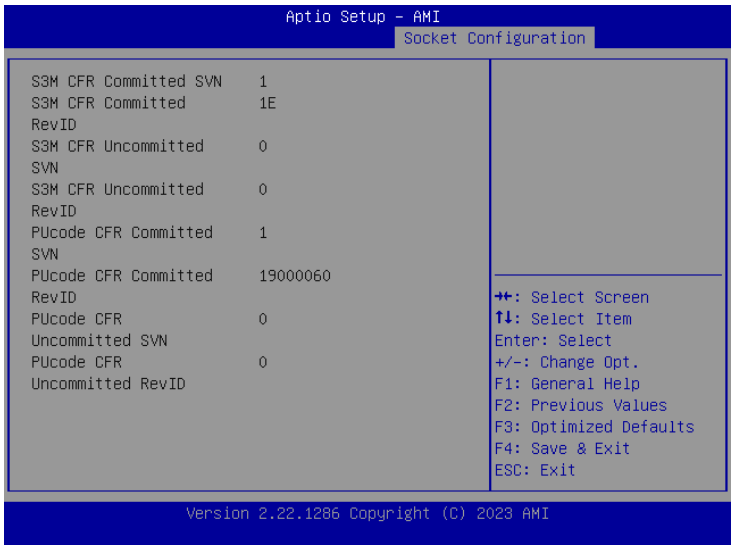
Manual Commit S3M FW CFR
Enable or disable the Manual Commit S3M FW CFR.

Provision PUcode CFR
Enable or disable the Provision PUcode CFR.

Manual Commit CFR PUcode CFR
Enable or disable the Manual Commit CFR PUcode CFR.

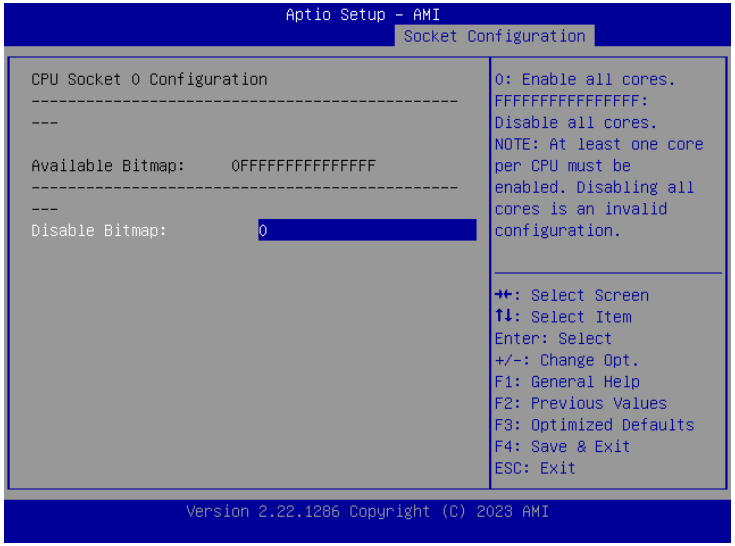
Socket 0/1/2/3 CFR Revision Info
Enters Socket 0/1/2/3 CFR Revision Info submenu.

Socket Configuration > Processor Configuration > Processor CFR Configuration > Socket 0/1/2/3 CFR Revision Info



Socket 0/1/2/3 CFR Revision Info
Display the information of Socket 0 ~ 3 CFR Revision.

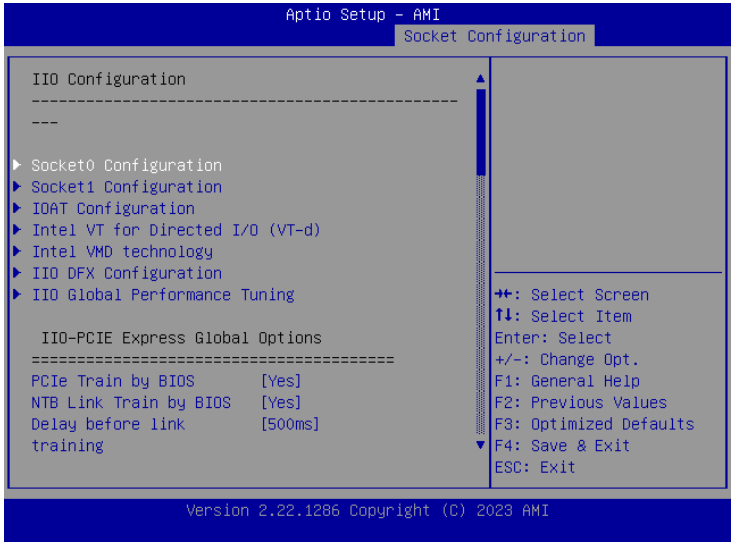
Socket Configuration > Processor Configuration > Per-Socket Configuration > CPU Socket 0/1 Configuration



Disable Bitmap

Provides the option to enable or disable all cores. 0 means enable all cores. FFFFFFFFFFFFFFF means disable all cores.

Socket Configuration > IIO Configuration



Socket0 Configuration
Enters Socket0 Configuration submenu.

Socket1 Configuration
Enters Socket1 Configuration submenu.

IOAT Configuration
Enters IOAT Configuration submenu.

Intel VT for Directed I/O (VT-d)
Enters Intel VT for Directed I/O (VT-d) submenu.

Intel VMD technology
Enters Intel VMD technology submenu.

IIO DFX Configuration
Enters IIO DFX Configuration submenu.

IIO Global Performance Tuning
Enters IIO Global Performance Tuning submenu.

PCIe Train by BIOS
Configures the Train by BIOS.

NTB Link Train by BIOS
Configures the NTB Link Train by BIOS.

Delay before link training
Configures the Delay before link training.

PCIe Hot Plug
Configures the PCIe Hot Plug.

CbDma MultiCast Enable
Configures the CbDma MultiCast Enable.

MultiCast Enable
Configures the MultiCast Enable.

NoSnoop Read Config
Enables or disables the NoSnoop Read Config.

NoSnoop Write Config
Enables or disables the NoSnoop Write Config.

Force NoSnoop Write Config
Enables or disables the Force NoSnoop Write Config.

Max Read Comp Comb Size
Configures the Max Read Comp Comb Size.

Problematic port
Enables or disables the Problematic port.

DMI Allocating Write Flows
Configures the DMI Allocating Write Flows.

PCIe Allocating Write Flows
Configures the PCIe Allocating Write Flows.

Skip Halt On DMI Degradation
Configures the Skip Halt On DMI Degradation.

Rx Clock WA
Enables or disables the Rx Clock WA.

Hide PCU Func 6
Configures the Hide PCU Func 6.

EN1K
Configures the EN1K.

Dual CV IO Flow
Configures the Dual CV IO Flow.

PCIE Coherent Read Full
Configures the PCIE Coherent Read Full.

PCI-E Completion Timeout
Configures the PCI-E Completion Timeout

PCI-E Completion Timeout
Configures the PCI-E Completion Timeout

PCI-E ASPM Support (Global)
Enables or disables the ASPM support for all downstream devices.

Snoop Response Hold off for PCIe Stack
Configures the Snoop Response Hold off for PCIe Stack.

Snoop Response Hold off for IOAT Stack
Configures the Snoop Response Hold off for IOAT Stack.

PCIe LTR Support
Configures the PCIe LTR Support.

PCIe Extended Tag Support
Configures the PCIe Extended Tag Support.

PCIe 10-bit Tag Support
Configures the PCIe 10-bit Tag Support.

PCIe Atomic Op Support
Configures the PCIe Atomic Op Support.

PCIe Max Read Request Size
Configures the PCIe Max Read Request Size.

PCIe PTM Support
Configures the PCIe PTM Support.

PCIe Relaxed Ordering
Configures the PCIe Relaxed Ordering.

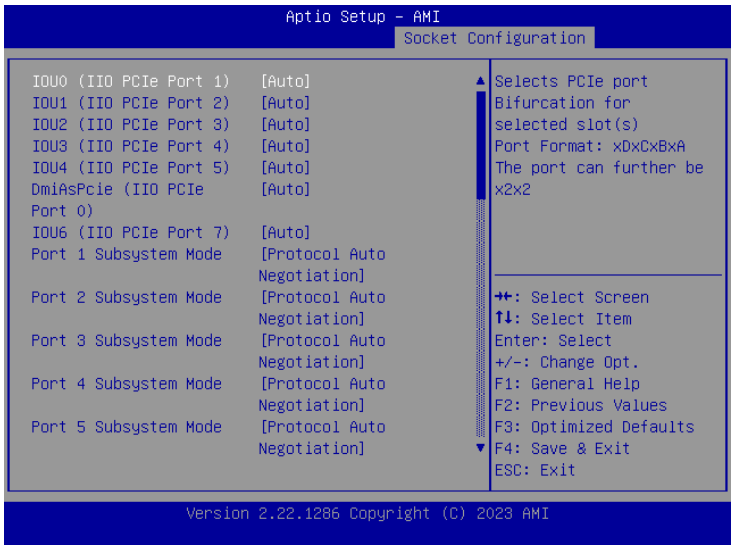
PCIe PHY Test mode
Configures the PCIe PHY Test mode.

PCIe ENQCMD/ENQCMDS
Configures the PCIe ENQCMD/ENQCMDS.

Equalization Bypass To Highest Rate
Enables or disables the Equalization Bypass To Highest Rate.

PE3 Link Speed Control
Configures the PE3 Link Speed Control.

Socket Configuration > IIO Configuration > Socket0 / Socket1 Configuration



IOU0 (IIO PCe Port 1) to IOU6 (IIO PCe Port 7)
Port Bifurcation settings for IOU 0 to IOU 6.

Port 0~7 Subsystem Mode
Configures the Port Subsystem mode.

IIO PCIe VC1 Port Bitmap
Configures the IIO PCIe VC1 Port Bitmap.

Sck0 RP Correctable
Configures the Sck0 RP Correctable.

Err
Configures the Err.

Sck0 RP Correctable Err
Enters IIO DFX Configuration submenu.

Sck0 RP NonFatal Uncorrectable Err
Enables or disables non-fatal error interruption.

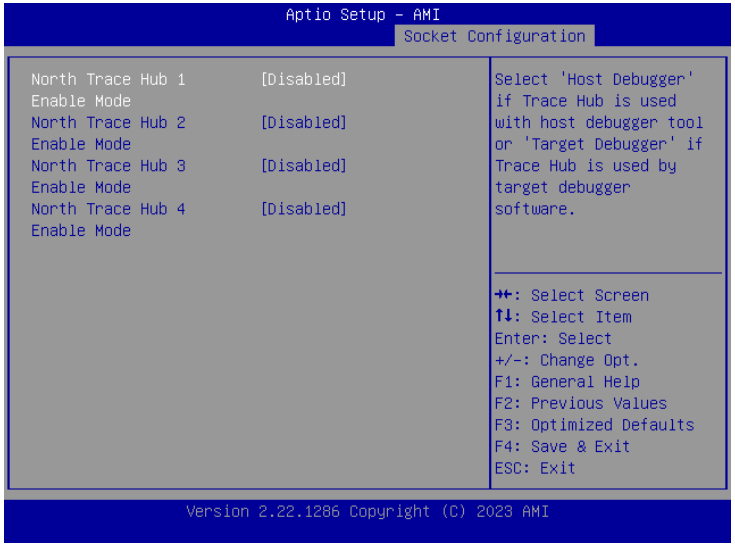
Sck0 RP Fatal Uncorrectable Err
Enable or disables fatal error interruption.

TraceHub Configuration Menu
Enters TraceHub Configuration submenu.

Port DMI
Enters DMI submenu.

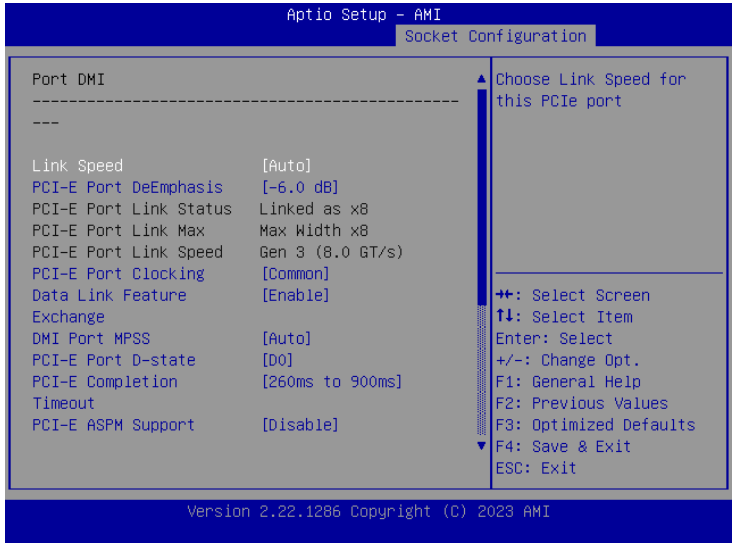
Port 1A / Port 1C / Port 1E / Port 1G / Port 2A / Port 2C / Port 2E / Port 2G / Port 3A / Port 3C / Port 3E / Port 3G / Port 4A / Port 4C / Port 4E / Port 4G / Port 5A / Port 5C / Port 5E / Port 5G
Presses to enter the relevant submenu.

Socket Configuration > IIO Configuration > Socket0 / Socket1 Configuration > TraceHub Configuration Menu



North Trace Hub 1~4 Enable Mode
Enables or disables the North Trace Hub 1~4 Enable Mode.

Socket Configuration > IIO Configuration > Socket0 / Socket1 Configuration > Port DMI



Link Speed
Configures the Link Speed mode.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the PCI-E Port Clocking.

Data Link Feature Exchange
Enables or disables the Data Link Feature Exchange.

DMI Port MPSS
Configures the DMI Port MPSS.

PCI-E Port D-state
Configures the PCI-E Port D-state.

PCI-E Completion Timeout
Configures the PCI-E Completion Timeout setting.

PCI-E ASPM Support
Enables or disables the PCI-E ASPM Support.

MSI
Enables or disables the MSI.

PCI-E Extended Sync
Configures the PCI-E Extended Sync.

Compliance Mode
Configures the Compliance Mode.

Unsupported Request
Enables or disables unsupported request reporting.

SRIS
Configures the SRIS.

ECRC Generation
Enables or disables ECRC Generation.

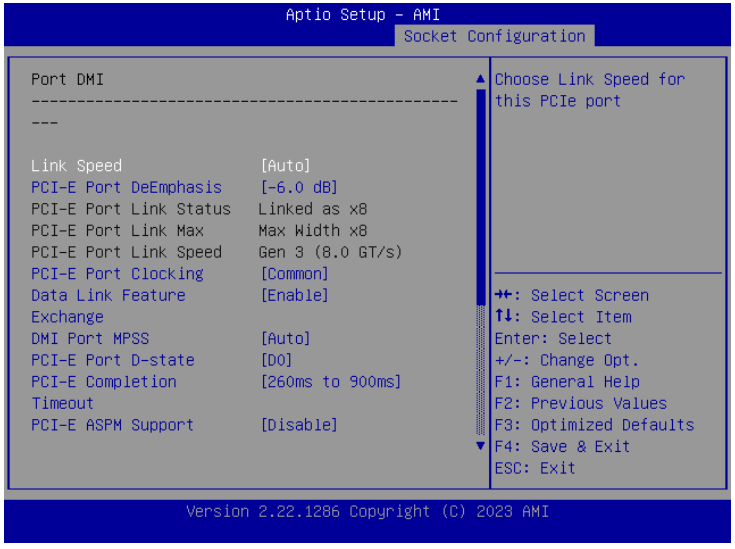
ECRC Check
Enables or disables ECRC Checking.

IODC Configuration
Configures the option for IODC (IO Direct Cache).

MCTP
Enables or disables MCTP.

Equalization Bypass to Highlight Rate
Enables or disables the Equalization Bypass to Highlight Rate.

Socket Configuration > IIO Configuration > Socket0 / Socket1 Configuration > Port 1A ~ Port 5G



PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

PCI-E Port Link Disable
Enables or disables link training of the PCIe port.

Link Speed
Configures the link speed of the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the PCI-E Port Clocking.

Data Link Feature Exchange
Enables or disables the Data Link Feature Exchange.

PCI-E Port MPSS
Configures the PCI-E Port MPSS.

PCI-E Port D-state
Configures the PCI-E Port D-state.

PCI-E Completion Timeout
Configures the PCI-E Completion Timeout setting.

PCI-E ASPM Support
Enables or disables the PCI-E ASPM Support.

MSI
Enables or disables the MSI.

PCI-E Extended Sync
Configures the PCI-E Extended Sync.

PCI-E 10-bit Tag Support
Configures the PCI-E 10-bit Tag Support.

PCI-E 10-bit Tag Support
Configures the PCI-E 10-bit Tag Support.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

Unsupported Request
Enables or disables unsupported request reporting.

SRIS
Configures the SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

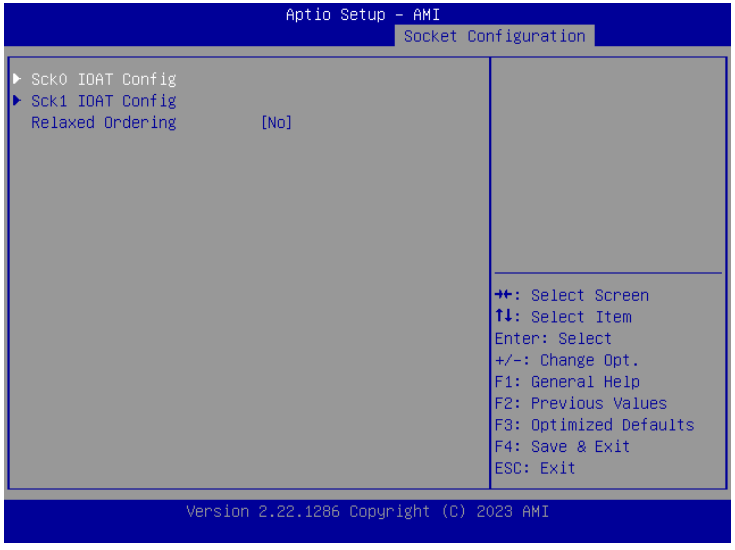
IODC Configuration
Configures the option for IODC (IO Direct Cache).

MCTP
Enables or disables MCTP.

Equalization Bypass to Highlight Rate
Enables or disables the Equalization Bypass to Highlight Rate.

CXL Drift Buffer
Enables or disables the CXL Drift buffer if there is a common reference clock.

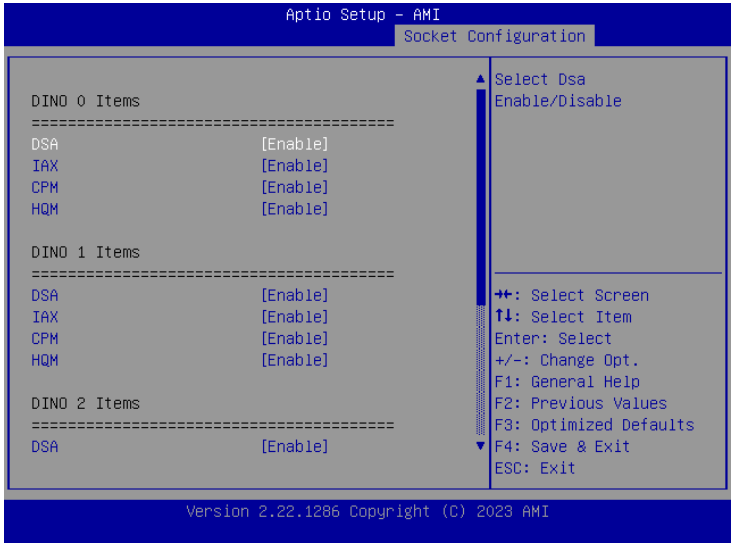
Socket Configuration > IIO Configuration > IOAT Configuration



Sck0 / Sck1 IOAT Config
Enters Sck0 / Sck1 IOAT Config submenu.

Relaxed Ordering
Configures the Relaxed Ordering.

Socket Configuration > IIO Configuration > IOAT Configuration > Sck0 / Sck1 IOAT Config



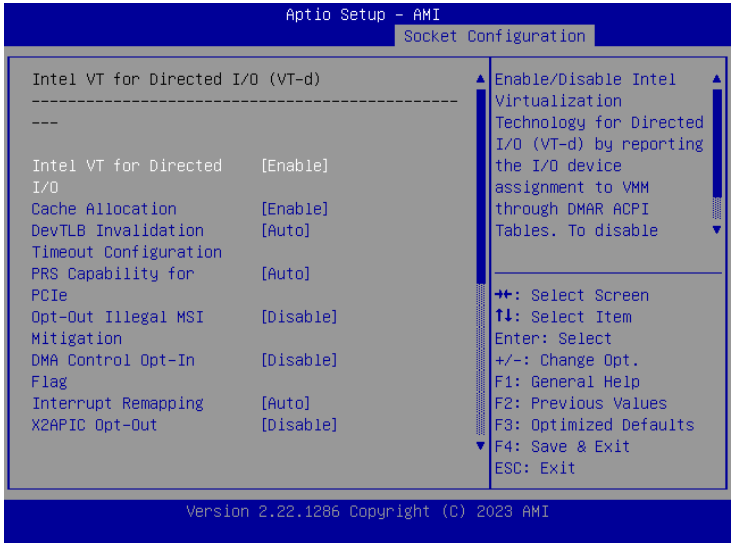
DINO 0 Items / DINO 1 Items / DINO 2 Items / DINO 3 Items
DSA
Enables or disables the DSA.

IAX
Enables or disables the IAX.

CPM
Enables or disables the CPM.

HQM
Enables or disables the HQM.

Socket Configuration > IIO Configuration > Intel VT for Directed IO (VT-d)



Intel VT for Directed I/O
Enables or disables Intel® Virtualization Technology for Directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI tables.

Cache Allocation
Enables or disables the Cache Allocation.

DevTLB Invlidation Timeout Configuration
Configures the DevTLB Invlidation Timeout Configuration.

PRS Capability for PCIe
Configures the PRS Capability for PCIe.

Opt-Out Illegal MSI Mitigation
Enables or disables the Opt-Out Illegal MSI Mitigation.

DMA Control Opt-In Flag
Enables or disables the DMA Control Opt-In Flag.

Interrupt Remapping
Configures the Interrupt Remapping.

X2APIC Opt-Out
Enables or disables the X2APIC mode.

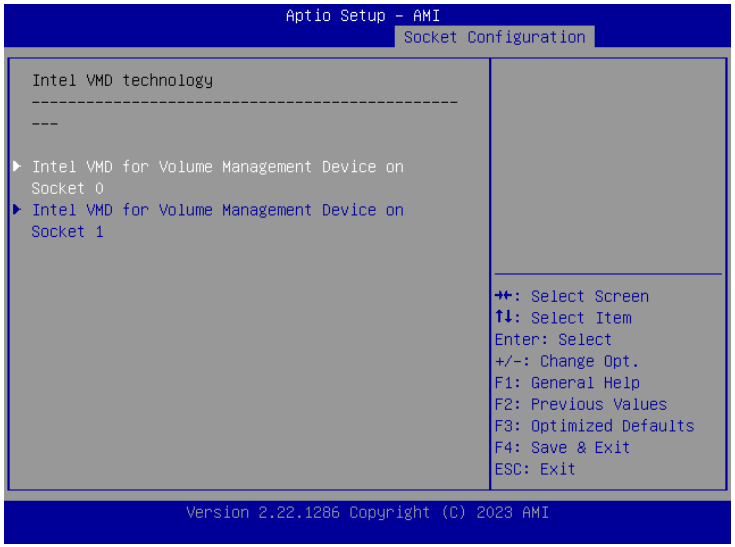
Pre-boot DMA Protection
Enables or disables the Pre-boot DMA Protection.

SATC Support
Enables or disables the SATC Support.

RHSA Support
Enables or disables the RHSA Support.

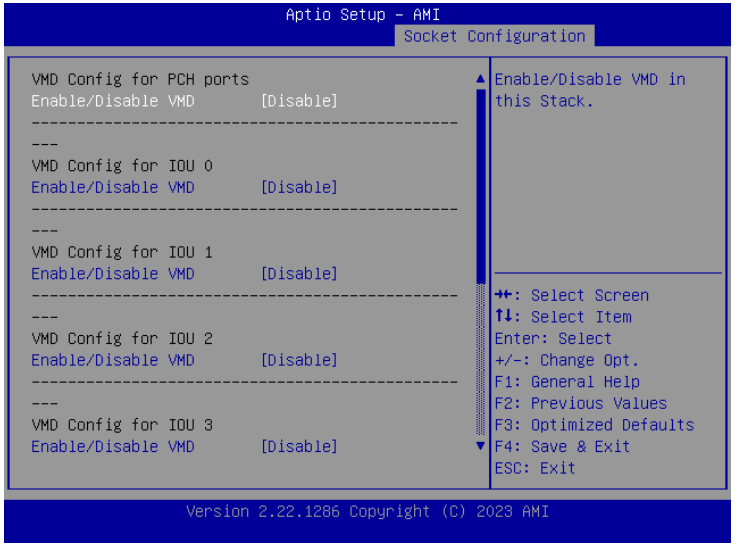
PCIe ACSCTL
Enables or disable soverwrite of PCI Access Control Services Control register in PCI root ports.

Socket Configuration > IIO Configuration > Intel VMD technology



Intel VMD for Volume Management Device on Socket 0 / Socket1
Enters Intel VMD for Volume Management Device on Socket 0 / Socket 1.

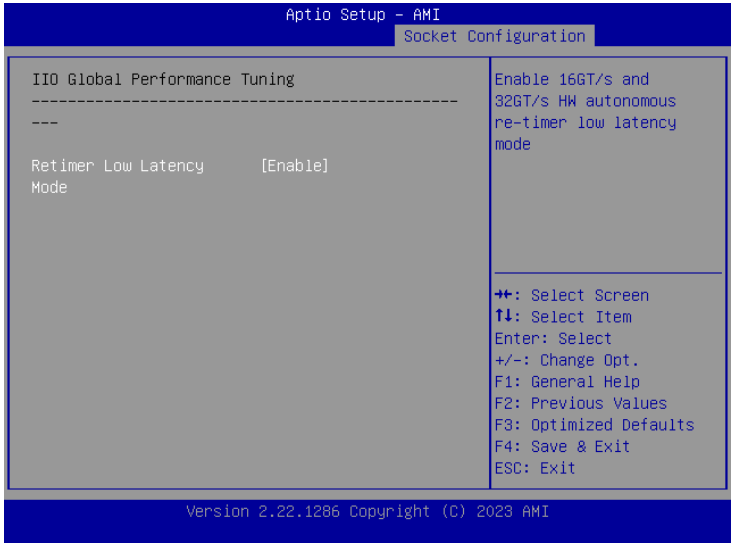
Socket Configuration > IIO Configuration > Intel VMD technology > Intel VMD for Volume Management Device on Socket 0 / Socket 1



Enable/Disable VMD
Enables or disables VMD in this Stack.

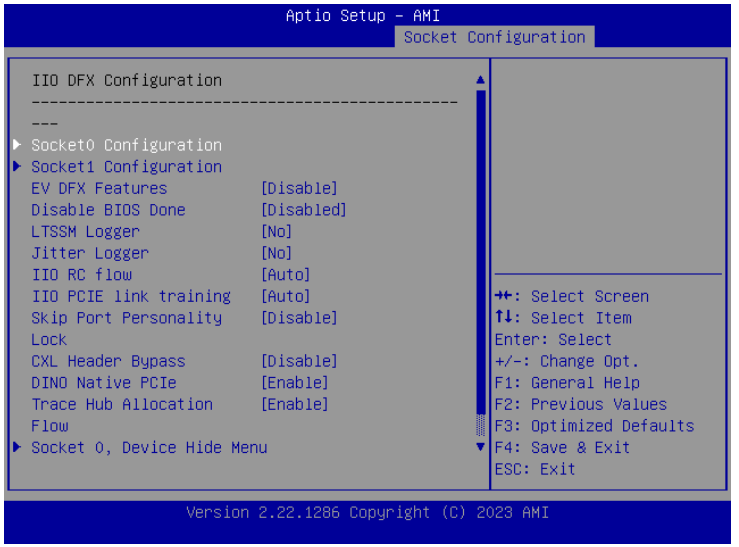
VMS Config for IOU 1~6
Enables or disables the VMD configuration for IOU 1~6.

Socket Configuration > IIO Configuration > IIO Global Performance Tuning



Retimer Low Latency Mode
Enables 16GT/s and 32GT/s HW autonomous re-timer low latency mode.

Socket Configuration > IIO Configuration > IIO DFX Configuration



Socket0 / Socket1 Configuration
Enters Socket0 / Socket1 Configuration submenu.

EV DFX Features
Enables or disables the DFX Lock Bits to remain clear.

Disable BIOS Done
Enables or disables the Disable BIOS Done.

LTSSM Logger
Configures the LTSSM Logger.

Jitter Logger
Configures the Jitter Logger.

IIO RC flow
Configures the IIO RC flow.

IIO PCIE link training
Configures the IIO PCIE link training.

Skip Port Personality Lock
Enables or disables the Skip Port Personality Lock.

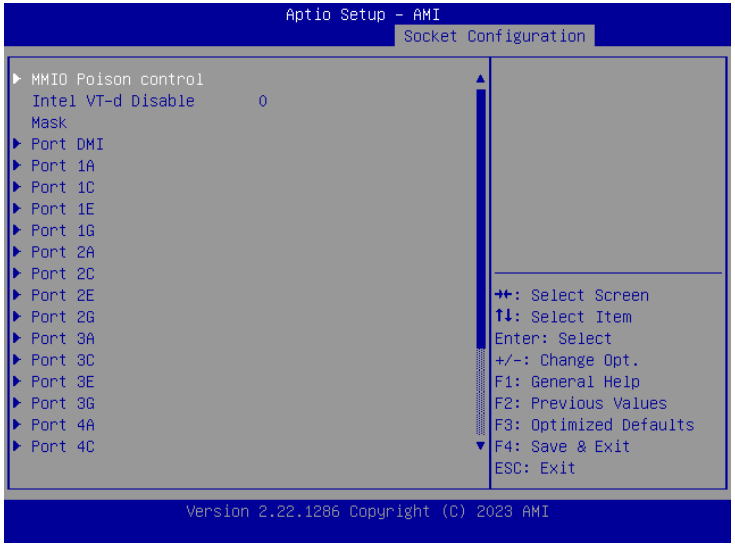
CXL Header Bypass
Enables or disables the CXL Header Bypass.

DINO Native Bypass
Enables or disables the DINO Native Bypass.

Trace Hub Allocation Flow
Enables or disables the Trace Hub Allocation Flow.

Socket0 / Socket1 Device Hide Menu
Enters Socket0 / Socket1 Device Hide submenu.

Socket Configuration > IIO Configuration > IIO DFX Configuration > Socket0 / Socket1 Configuration



MMIO Poision control
Enters MMIO Poision control submenu.

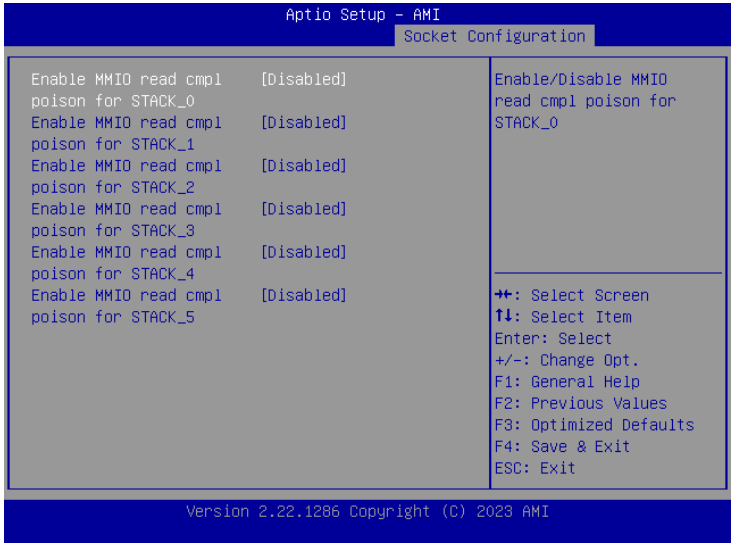
Intel VT-d Disable
Configures the Intel VT-d Disable.

Mask
Configures the Mask.

Port DMI
Enters Port DMI submenu.

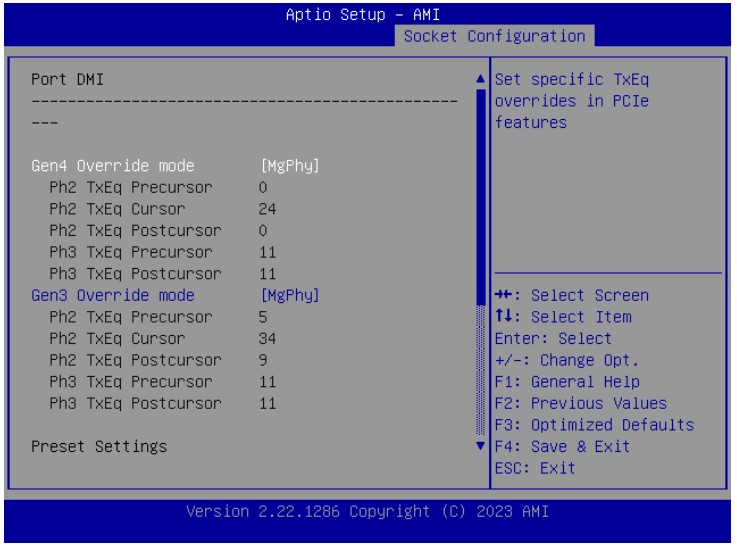
Port 1A / Port 1C / Port 1E / Port 1G / Port 2A / Port 2C / Port 2E / Port 2G / Port 3A / Port 3C / Port 3E / Port 3G / Port 4A / Port 4C / Port 4E / Port 4G / Port 5A / Port 5C / Port 5E / Port 5G
Presses to enter the relevant submenu.

Socket Configuration > IIO Configuration > IIO DFX Configuration > Socket0 / Socket1 Configuration > MMIO Poison control



Enable MMIO read cmpl poison for STACK_0 ~5
Enables or disables MMIO read cmpl poison for STACK_0 ~5.

Socket Configuration > IIO Configuration > IIO DFX Configuration > Socket0 / Socket1 Configuration > Port DMI



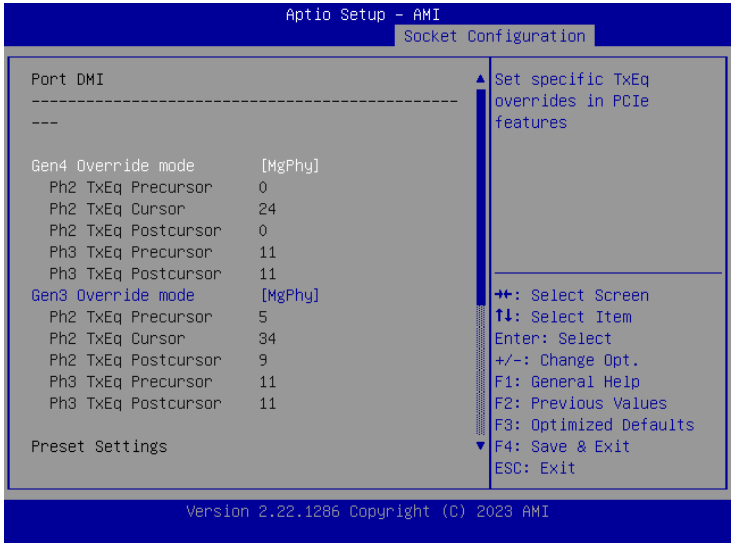
Gen4 / Gen3 Override mode
Sets specific TxEq overrides in PCIe features.

DN Tx Preset Gen3 ~ Gen5
Configures the DN Tx Preset Gen3 ~ Gen5.

UP Tx Preset Gen4
Configures the UP Tx Preset Gen4.

Link Re-Train
Enables or disables Link Re-Train if connected at degraded speed or width.

Socket Configuration > IIO Configuration > IIO DFX Configuration > Socket0 / Socket1 Configuration > Port 1A



CXL Debug mode
Enables or disables the CXL Debug mode.

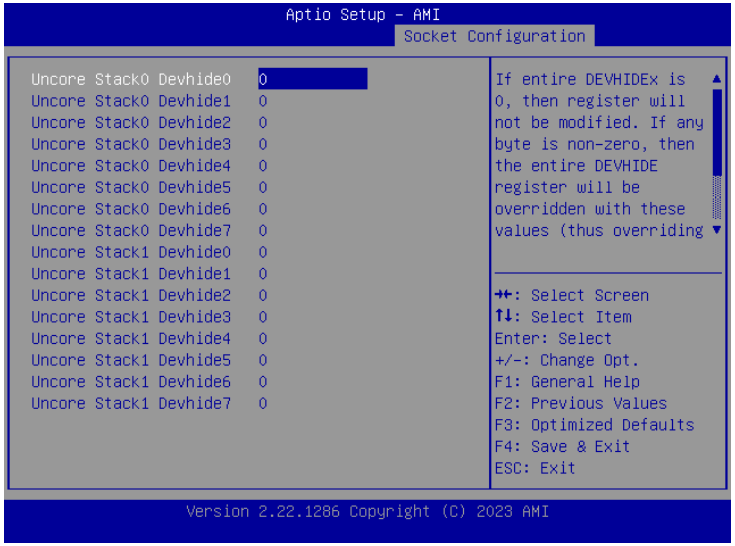
Gen5 ~ Gen 3 Override mode
Configures the Gen5 ~ Gen3 override mode.

DN Tx Preset Gen3 ~ Gen5
Configures the DN Tx Preset Gen3 ~ Gen5.

UP Tx Preset Gen4
Configures the UP Tx Preset Gen4.

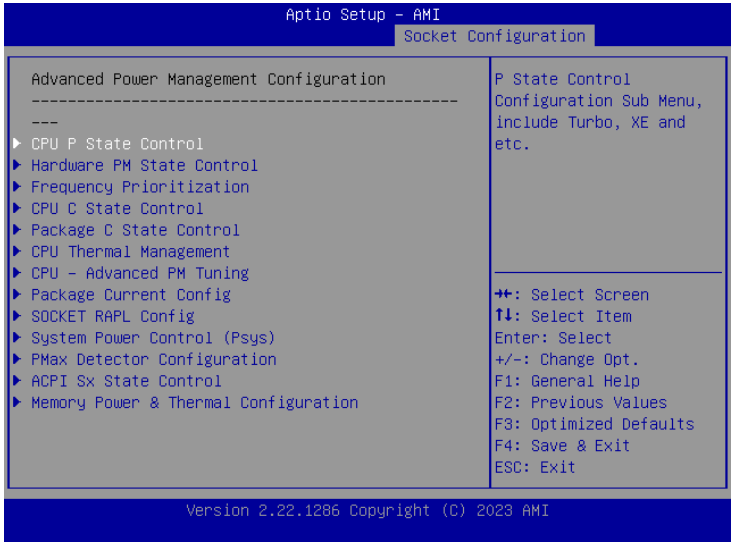
Link Re-Train
Enables or disables Link Re-Train if connected at degraded speed or width.

Socket Configuration > IIO Configuration > IIO DFX Configuration > Socket 0 / Socket 1, Device Hide Menu



Uncore Stack0 Devhide 0 ~7
Configures the Uncore Stack0 Devhide 0 ~7.

Socket Configuration > Advanced Power Management Configuration



CPU P State Control
Enters CPU P State Control submenu.

Hardware PM State Control
Enters Hardware PM State Control submenu.

Frequency Prioritization
Enters Frequency Prioritization submenu.

CPU C State Control
Enters CPU C State Control submenu.

CPU Thermal Management
Enters CPU Thermal Management submenu.

CPU - Advanced PM Tuning
Enters CPU - Advanced PM Tuning submenu.

Package Current Config
Enters Package Current Config submenu.

SOCKET RAPL Config
Enters SOCKET RAPL Config submenu.

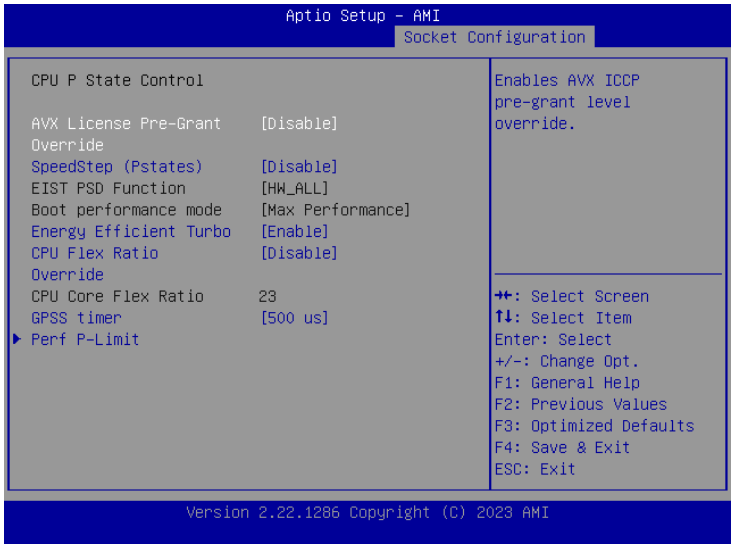
System Power Control (Psys)
Enters System Power Control (Psys) submenu.

PMax Detector Configuration
Enters PMax Detector Configuration submenu.

ACPI Sx State Control
Enters ACPI Sx State Control submenu.

Memory Power & Thermal Configuration
Enters Memory Power & Thermal Configuration submenu.

Socket Configuration > Advanced Power Management Configuration > CPU P State Control



AVX Licencse Pre-Grant Override
Enables or disables AVX ICCP pre-grant level override.

SpeedStep (Pstates)
Enables or disables Intel® SpeedStep technology.

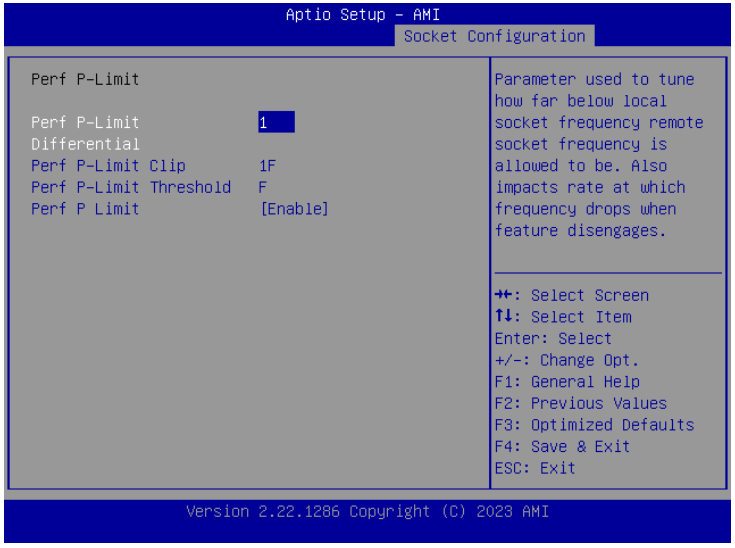
Energy Efficient Turbo
Enables or disables the Energy Efficient Turbo.

CPU Flex Ratio Override
Enables or disables CPU Flex Ratio Override.

GPSS Timer
Configures the GPSS Timer value.

Perf P-Limit
Enters Perf P-Limit submenu.

Socket Configuration > Advanced Power Management Configuration > CPU P State Control > Perf P-Limit



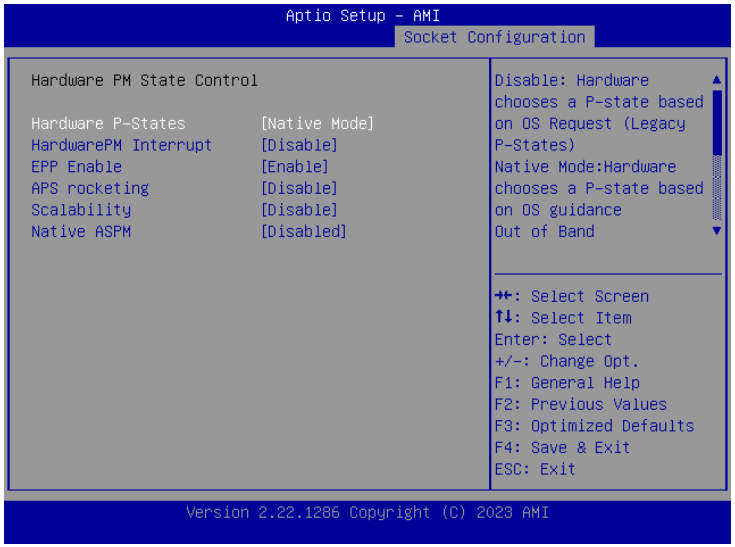
Perf P-Limit Differential
Parameter used to tune how far below local socket frequency remote socket frequency is allowed to be. Also impacts the rate at which the frequency drops when feature disengages.

Perf P-Limit Clip
Configures the performance P-Limit Clip value.

Perf P-Limit Threshold
Configures the performance P-Limit Threshold value.

Perf P Limit
Enables or disables performance P Limit.

Socket Configuration > Advanced Power Management Configuration > Hardware PM State Control



Hardware P-States

Disable	Hardware chooses a P-state based on OS Request. (Legacy P-States).
Native Mode	Hardware chooses a P-state based on OS guidance.
Out of Band	Mode Hardware autonomously chooses a P-state (no OS guidance).

HardwarePM Interrupt

Enables or disables the HardwarePM Interrupt.

EPP Enable

Enables or disables the EPP feature.

APS rocketing

Enables or disables the APS rocketing

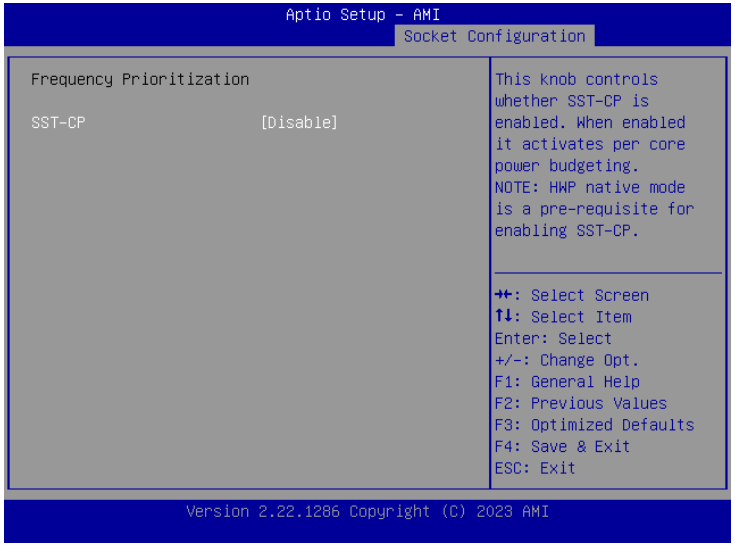
Scalability

Enables or disables the Scalability.

Native ASPM

Enables or disables the Native ASPM.

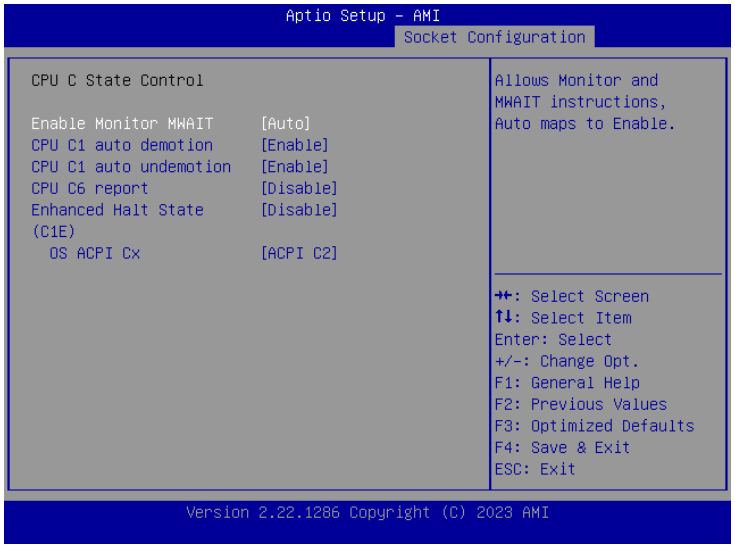
Socket Configuration > Advanced Power Management Configuration > Frequency Prioritization



SST-CP

This knob controls whether SST-CP is enabled. When enabled it activates per core power budgeting. Note: HWP native mode is a pre-requisite for enabling SST-CP.

Socket Configuration > Advanced Power Management Configuration > CPU C State Control



Enabled Monitor MWAIT
Allow Monitor and MWAIT instructions, Auto maps to enable.

CPU C1 auto demotion
Enables or disables the CPU C1 auto demotion.

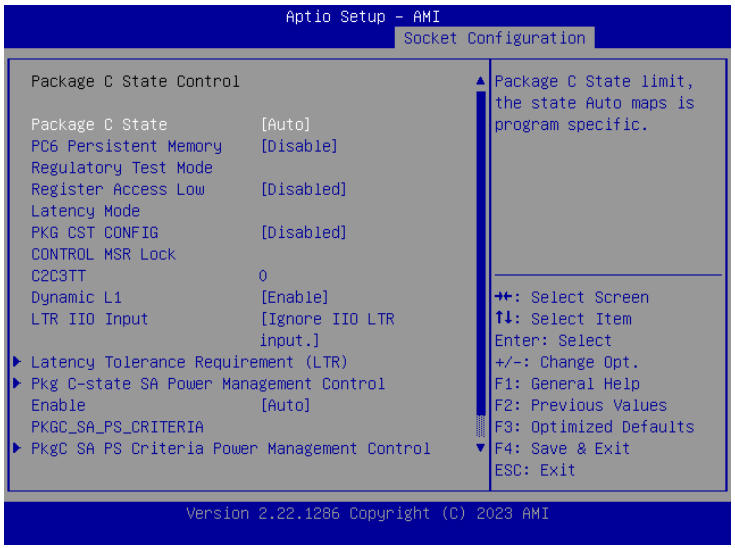
CPU C1 auto undemotion
Enables or disables the CPU C1 auto undemotion.

CPU C6 report
Enables or disables the C6 report to the operating system.

Enhanced Halt State (C1E)
Enables or disables the Enhanced Halt State (C1E) for lower power consumption.

OS ACPI Cx
Enables or disables the C3 report or C6 report to OS ACPI C2 or ACPI C3.

Socket Configuration > Advanced Power Management Configuration > Package C State Control



Package C State
Package C State limit, the state Auto maps is program specific.

PC6 Persistent Memory Regulator Test Mode
Enables or disables the PC6 Persistent Memory Regulator Test Mode.

Register Access Low Latency Mode
Enables or disables the Regulator Test Mode Register Access Low Latency Mode.

PKG CST CONFIG CONTROL MSR Lock
Enables or disables the PKG CST Config Control MSR Lock.

C2C3TT
Enables or disables the C2C3TT.

Dynamic L1
Enables or disables the Dynamic L1.

LTR IIO Input
Enables or disables the Dynamic L1.

Latency Tolerance Requirement (LTR)
Enters Latency Tolerance Requirement (LTR) submenu.

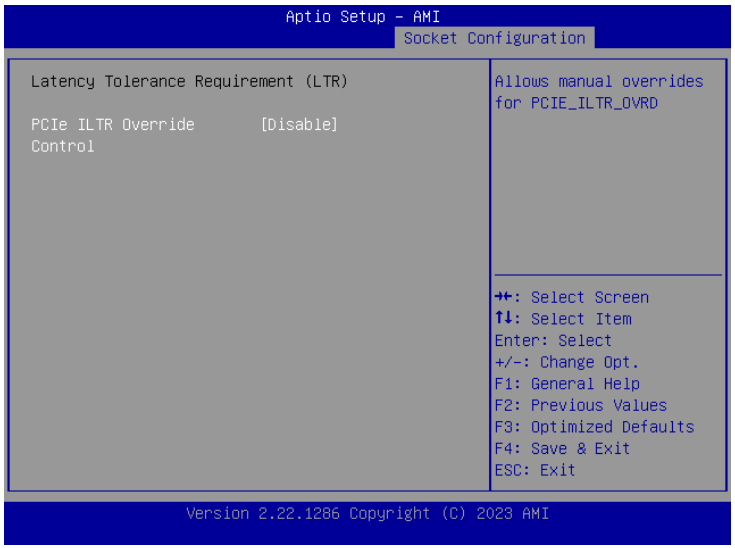
Pkg C-state SA Power Management Control
Enters Pkg C-state SA Power Management Control submenu.

Enable PKGC_SA_PS_Criteria
Enables or disables the Enable PKGC_SA_PS_Criteria.

PkgC SA PS Criteria Power Management Control
Enters PkgC SA PS Criteria Power Management Control submenu.

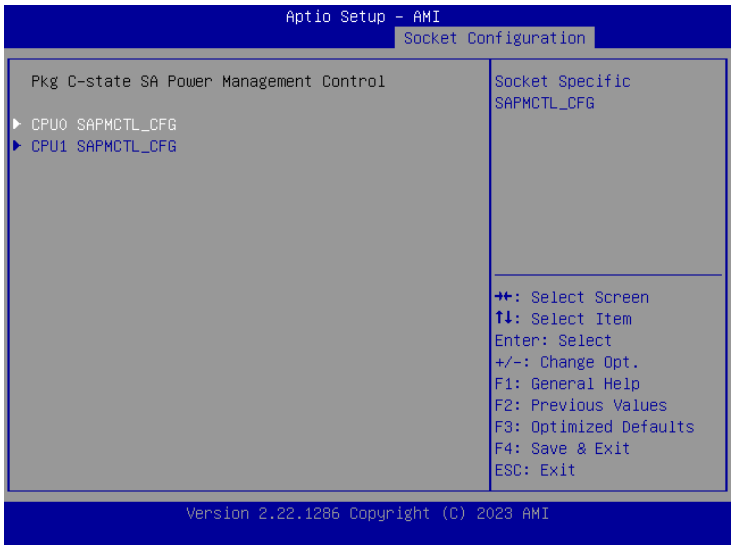
PKGc Interrupt Response Time
Enters PKGc Interrupt Response Time submenu.

Socket Configuration > Advanced Power Management Configuration > Package C State Control > Latency Tolerance Requirement (LTR)



PCIe ILTR Override Control
Allows manual overrides for PCIE_ILTR_OVRD.

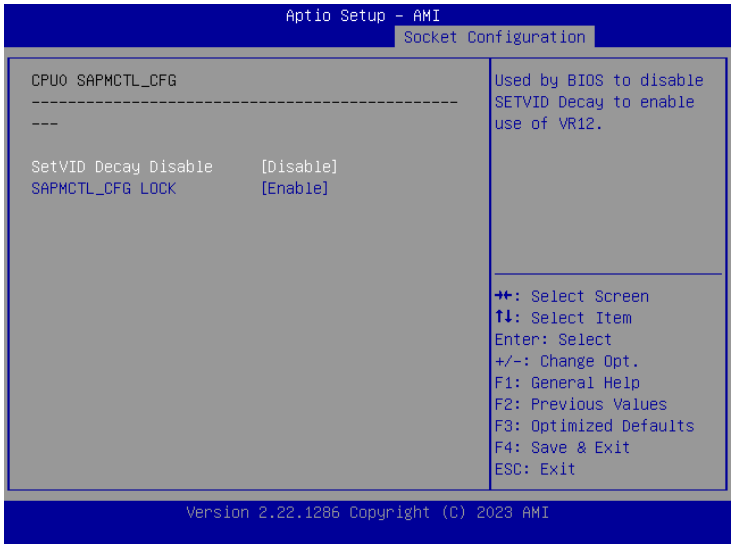
Socket Configuration > Advanced Power Management Configuration > Package C State Control > Pkg C-state SA Power Management Control



CPU0 SAPMCTL_CFG
Enters CPU0 SAPMCTL_CFG submenu.

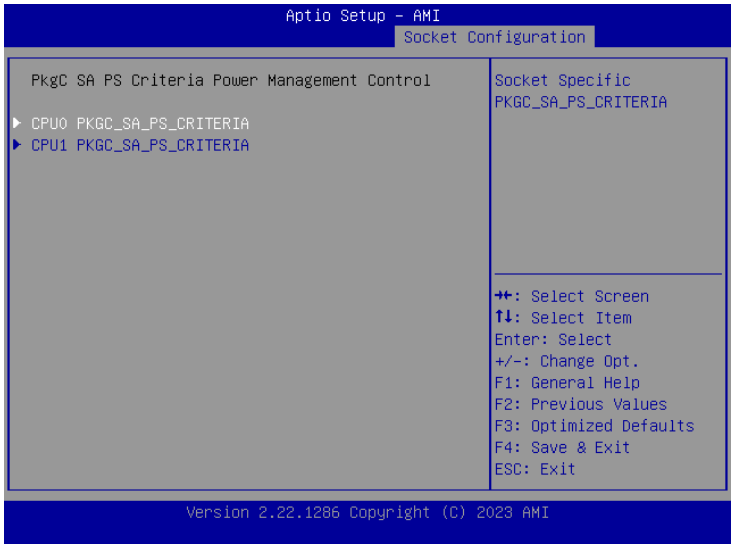
CPU1 SAPMCTL_CFG
Enters CPU0 SAPMCTL_CFG submenu.

Socket Configuration > Advanced Power Management Configuration > Package C State Control > Pkg C-state SA Power Management Control > CPU0 / CPU1 SAPMCTL_CFG



SetVID Decay Disable
Used by BIOS to disable SETVID Decay to enable use of VR12.

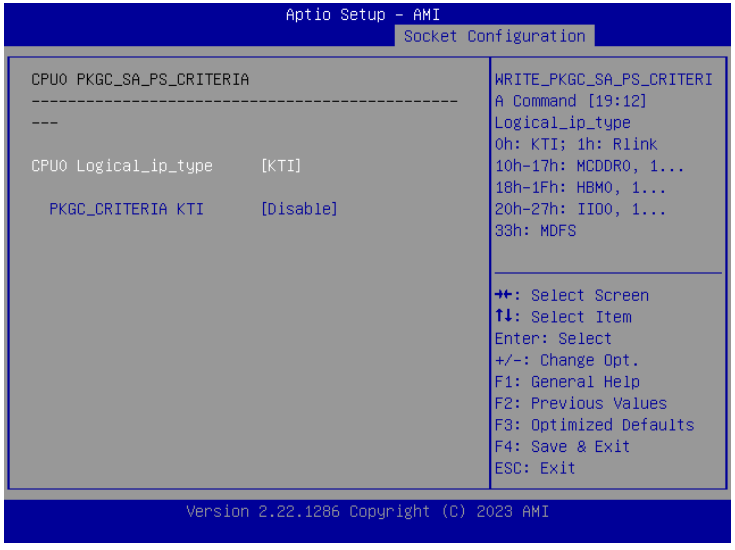
Socket Configuration > Advanced Power Management Configuration > Package C State Control > PkgC SA PS Criteria Power Management Control



CPU0 PKGC_SA_PS_CRITERIA
Enters CPU0 PKGC_SA_PS_CRITERIA submenu.

CPU1 PKGC_SA_PS_CRITERIA
Enters CPU0 PKGC_SA_PS_CRITERIA submenu.

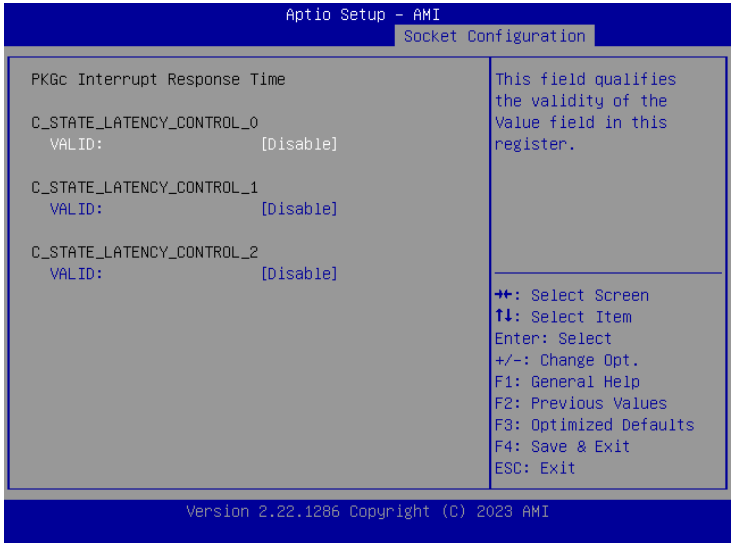
Socket Configuration > Advanced Power Management Configuration > Package C State Control > PkgC SA PS Criteria Power Management Control > CPU0 / CPU1 PKGC_SA_PS_CRITERIA



CPU0 Logical_ip_type
Configures the CPU0 Logical_ip_type.

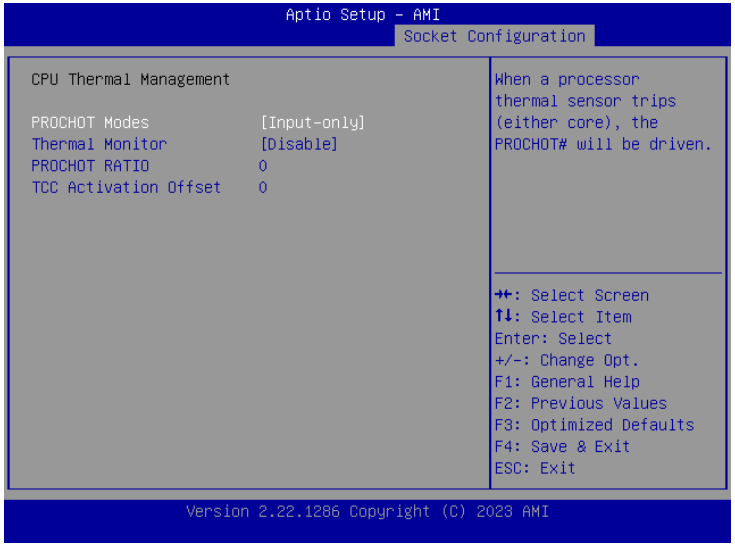
PKGC_CRITERIA KTI
Enables or disables the PKGC_CRITERIA KTI.

Socket Configuration > Advanced Power Management Configuration > Package C State Control > PkgC SA PS Criteria Power Management Control > PKGc Interrupt Response Time



C_STATE_LATENCY_CONTROL_0 / 1 / 2
This field qualifies the validity of the value field in this register.

Socket Configuration > Advanced Power Management Configuration > CPU Thermal Management



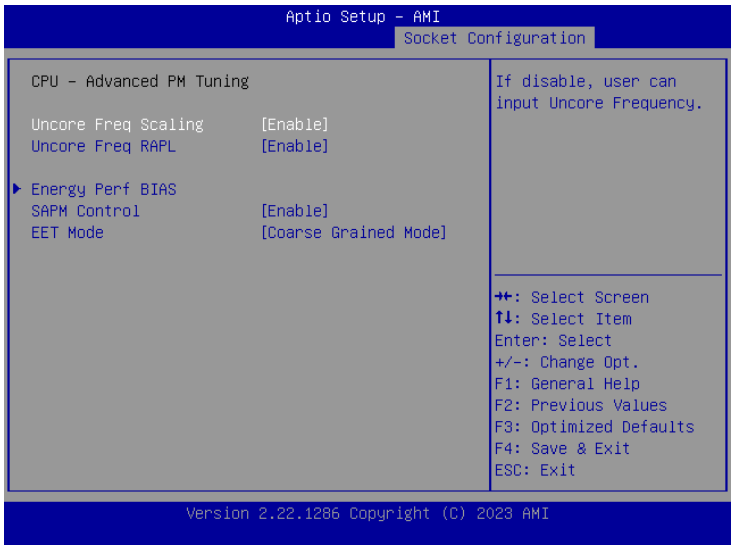
PROCHOT Modes
When a processor thermal sensor trips (either core), the PROCHOT# will be driven.

Thermal Monitor
Enables or disables the Thermal Monitor.

PROCHOT RATIO
Configures the PROCHOT RATIO.

TCC Activation Offset
Configures the TCC Activation Offset.

Socket Configuration > Advanced Power Management Configuration > CPU - Advanced PM Tuning



Uncore Freq Scaling
If disable, use can input Uncore Frequency.

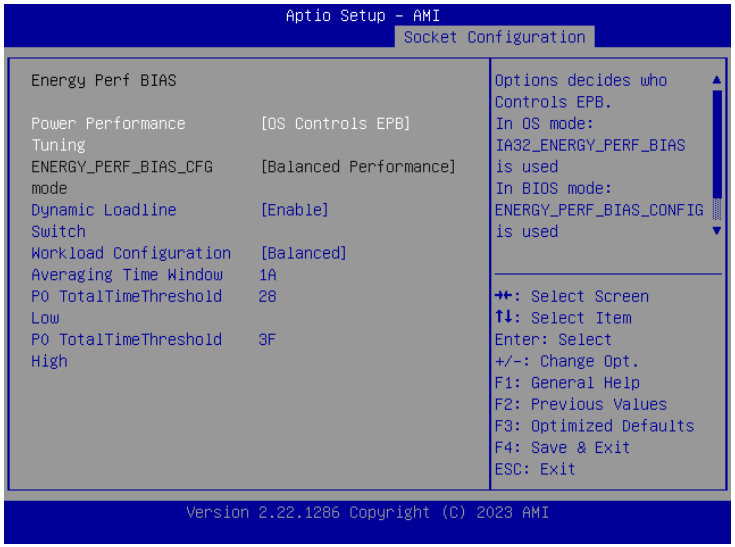
Uncore Freq RAPL
Enables or disables the Uncore Freq RAPL.

Energy Perf BIAS
Enters Energy Perf BIAS submenu.

SAPM Control
Enables or disables the SAPM Control.

EET Mode
Configures the EET Mode.

Socket Configuration > Advanced Power Management Configuration > CPU - Advanced PM Tuning > Energy Perf BIAS



Power Performance Tuning
Configures whether to allow the BIOS or OS to control the power performance tuning.

Dynamic Loadline Switch
Enables or disables the Dynamic Loadline Switch.

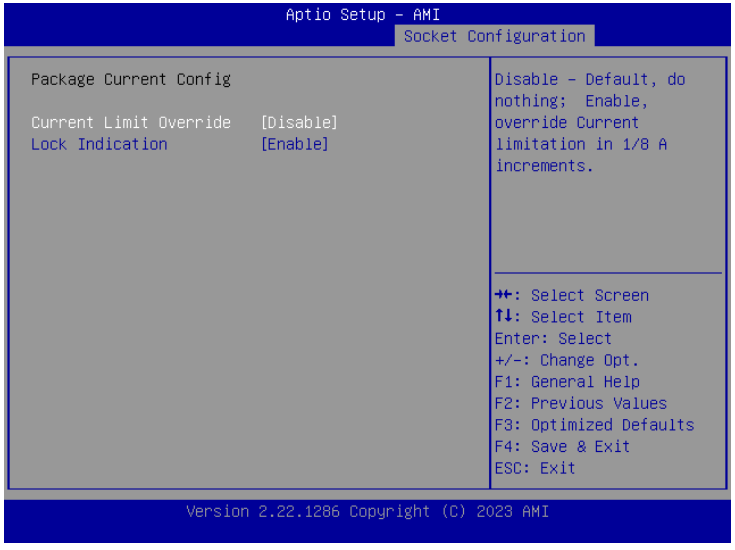
Workload Configuration
Configures the Workload Configuration.

Averaging TIme Window
Configures the Averaging Time Window.

P0 TotalTimerThreshold Low
Configures the P0 TotalTimerThreshold Low.

P0 TotalTimerThreshold High
Configures the P0 TotalTimerThreshold High.

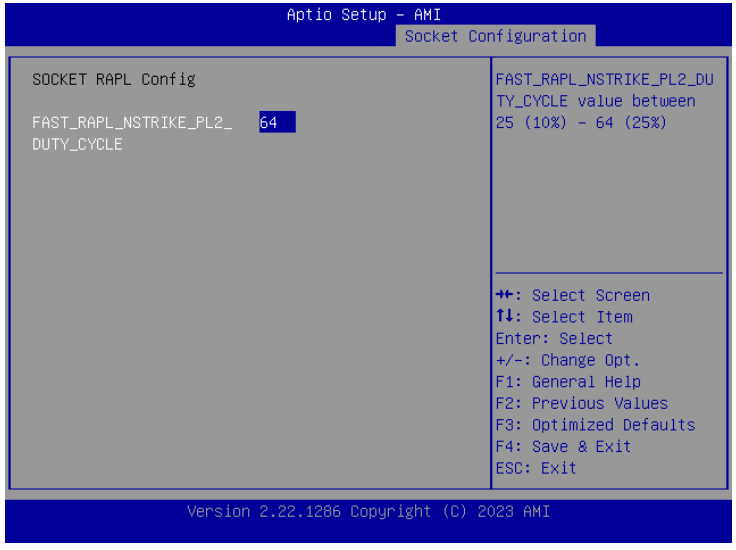
Socket Configuration > Advanced Power Management Configuration > Package Current Config



Current Limit Override
When enabled, overrid current limition in 1/8 A increments, By default, it's disabled, do nothing.

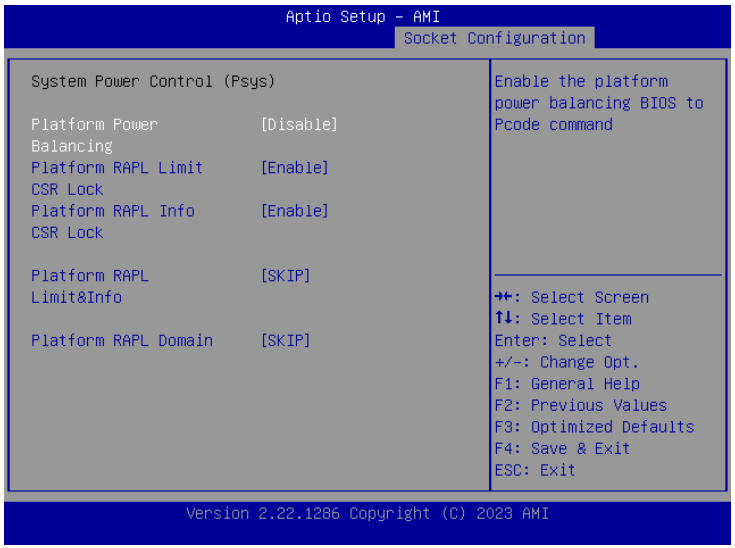
Lock Indication
Enables or disables the Lock indication.

Socket Configuration > Advanced Power Management Configuration > SOCKET RAPL Config



FAST_RAPL_NSTRIKE_PL2_DUTY_CYCLE
FAST_RAPL_NSTRIKE_PL2_DUTY_CYCLE value is between 25 (10%) - 64 (25%).

Socket Configuration > Advanced Power Management Configuration > System Power Control (Psys)



Platform Power Balancing
Enables the platform power balancing BIOS to Pcode command.

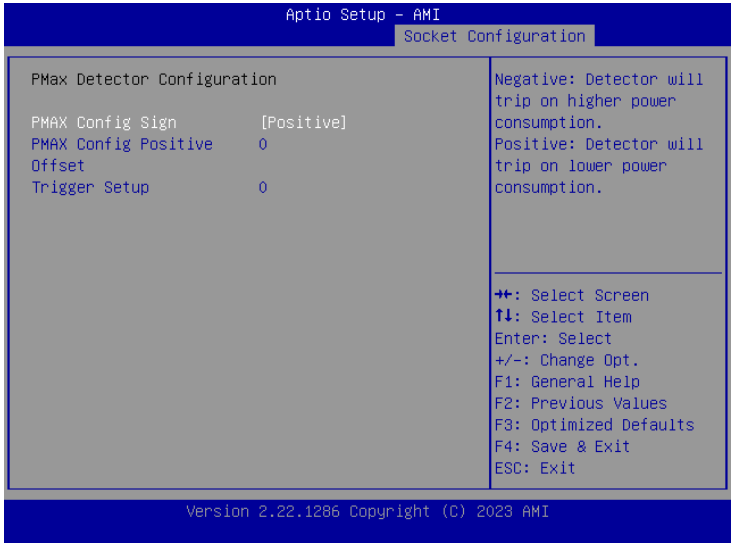
Platform RAPL Limit CSR Lock
Enables or disables the Platform RAPL Limit CSR Lock.

Platform RAPL Info CSR Lock
Enables or disables the Platform RAPL Info CSR Lock.

Platform RAPL & Info
Configures the Platform RAPL & Info.

Platform RAPL Domain
Configures the Platform RAPL Domain.

Socket Configuration > Advanced Power Management Configuration > PMax Detector Configuration

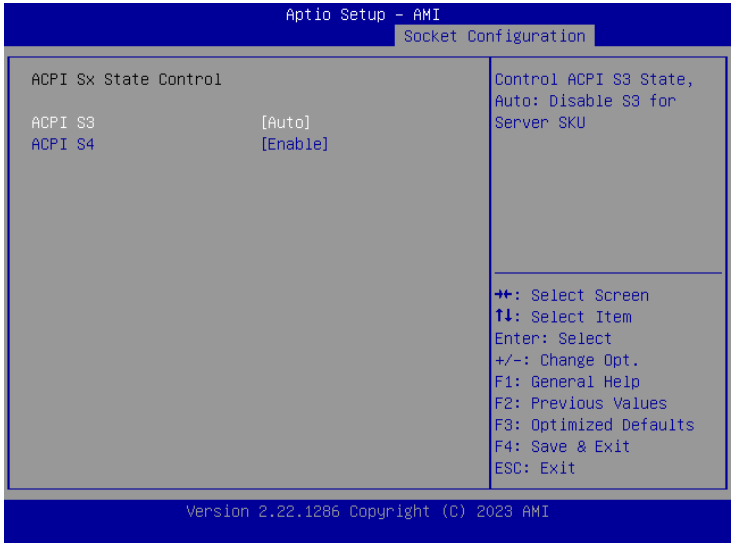


PMax Config Sign
Configures the PMax Config Sign.
Negative: Detector will trip on higher power consumption.
Positive: Detector will trip on lower power consumption.

Pmax Config Positive Offset
Configures the Pmax Config Positive Offset.

Trigger Setup
Configures the Trigger Setup.

Socket Configuration > Advanced Power Management Configuration > ACPI Sx State Control

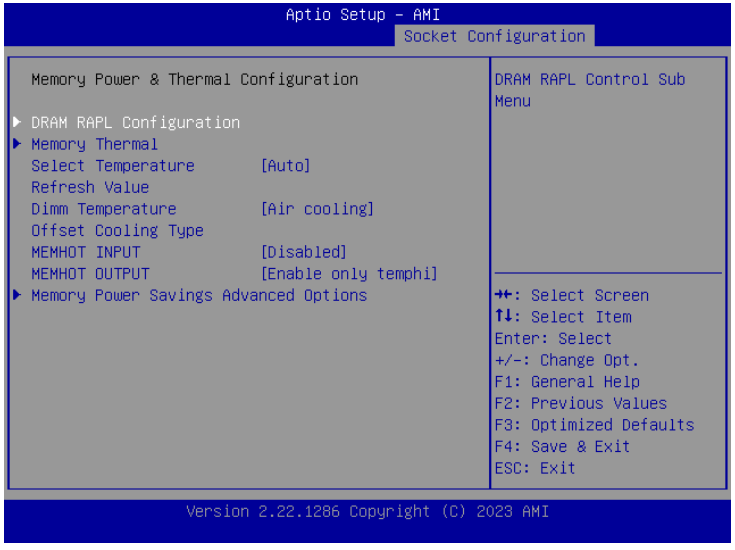


ACPI S3
Contols ACPI S3 State. Auto: Disable S3 for server SKU

ACPI S4
Enables or disables the APCI S4.

Trigger Setup
Configures the Trigger Setup.

Socket Configuration > Advanced Power Management Configuration > Memory Power & Thermal Configuration



DRAM RAPL Configuration
Enters DRAM RAPL Configuration submenu.

Memory Thermal
Enters Memory Thermal submenu.

Select Temperature Refresh Value
Configures the Select Temperature Refresh Value.

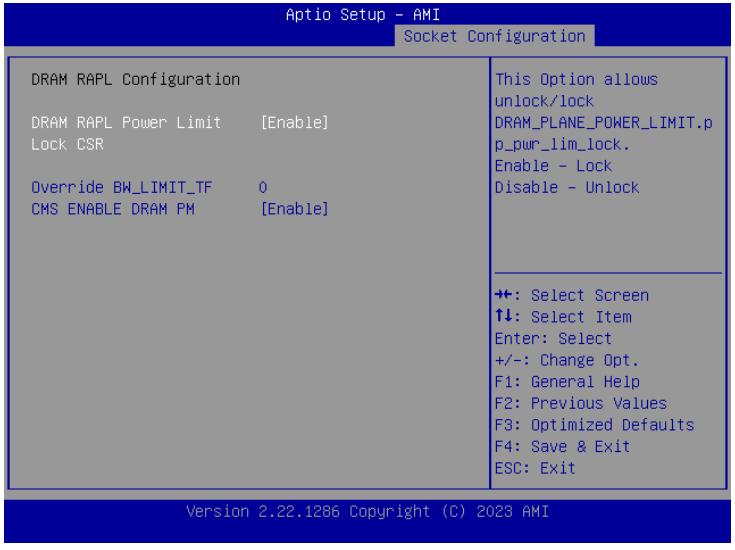
Dimm Temperature Offset Cooling Type
Configures the Dimm Temperature Offset Cooling Type.

MEMHOT INPUT
Enables or disables the MEMHOT INPUT.

MEMHOT OUTPUT
Enables or disables the MEMHOT OUTPUT.

Memory Power Savings Advanced Options
Enters Memory Power Savings Advanced Options submenu.

Socket Configuration > Advanced Power Management Configuration > Memory Power & Thermal Configuration > DRAM RAPL Configuration

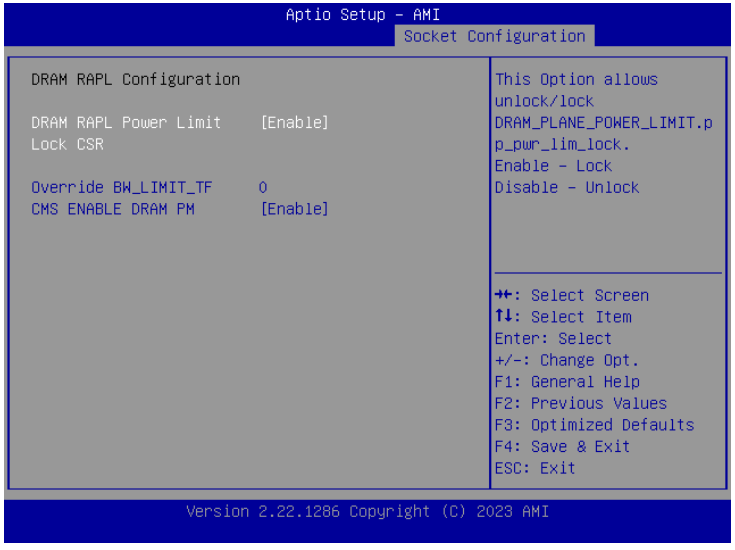


DRAM RAPL Power Limit Lock CSR
This option allows unlock/lock DRAM_PLANE_POWER_LIMIT.pp_pwr_lim_lock.
Enable: Lock
Disable: Unlock.

Override BW_LIMIT_TF
Configures the Override BW_LIMIT_TF.

CMS ENABLE DRAM PM
Enables or disbles the CMS ENABLE DRAM PM.

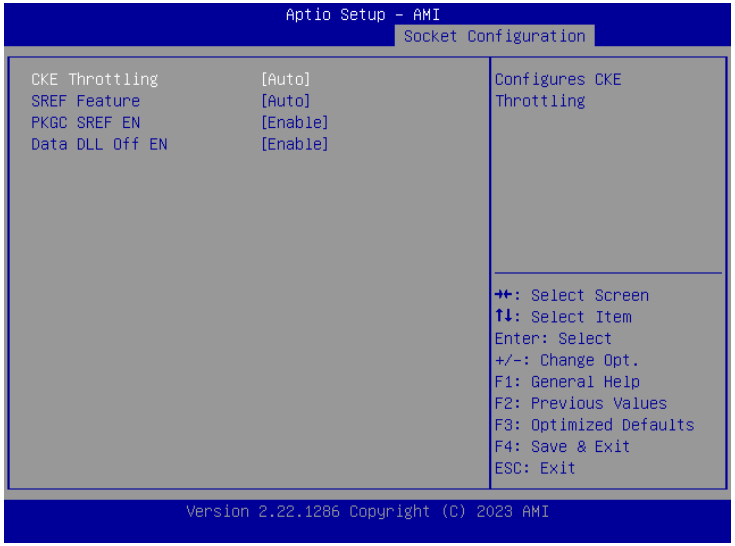
Socket Configuration > Advanced Power Management Configuration > Memory Power & Thermal Configuration > Memory Thermal



Throtting Mode
Configures Thermal Throtting Mode.

MEMTRIP REPORTING
Enables or disables the MEMTRIP REPORTING.

Socket Configuration > Advanced Power Management Configuration > Memory Power & Thermal Configuration > Memory Power Savings Advanced Options



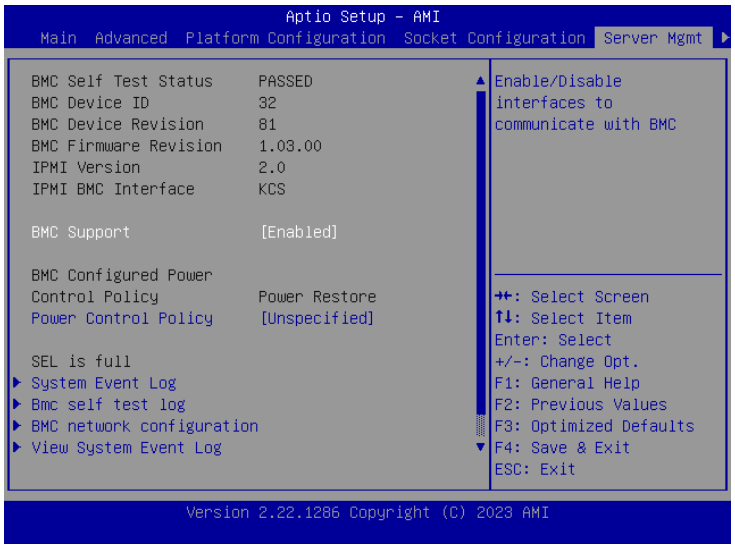
CKE Throttling
Configures CKE Throttling.

SREF Feature
Configures SREF Feature.

PKGC SREF EN
Enables or disables the PKGC SREF EN.

Data DLL Off EN
Enables or disables the Data DLL Off EN.

Server Mgmt



BMC Support
Enable or disable interfaces to communicate with the BMC.

Power Control Policy
Configures the Power Control Policy.

System Event Log
Enters the System Event Log submenu.

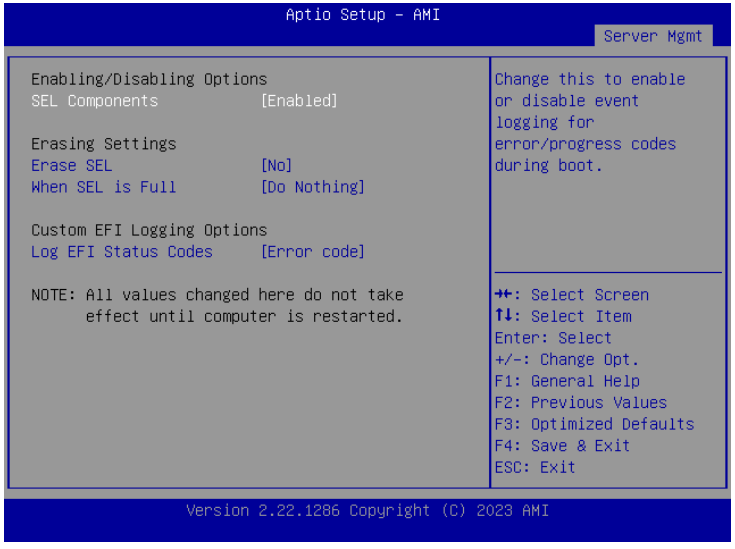
Bmc self test log
Enters the Bmc self test log submenu.

BMC network configuration
Enters the BMC network configuration submenu.

View Systew Event Log
Enters the View Systew Event Log submenu.

Server Mgmt > Systen Event Log

Note: All values changed here will not take effect until computer is restarted.



SEL Components

Changes this to enable or disable event logging for error/progress codes during boot.

Erase SEL

Configures the options for erasing SEL.

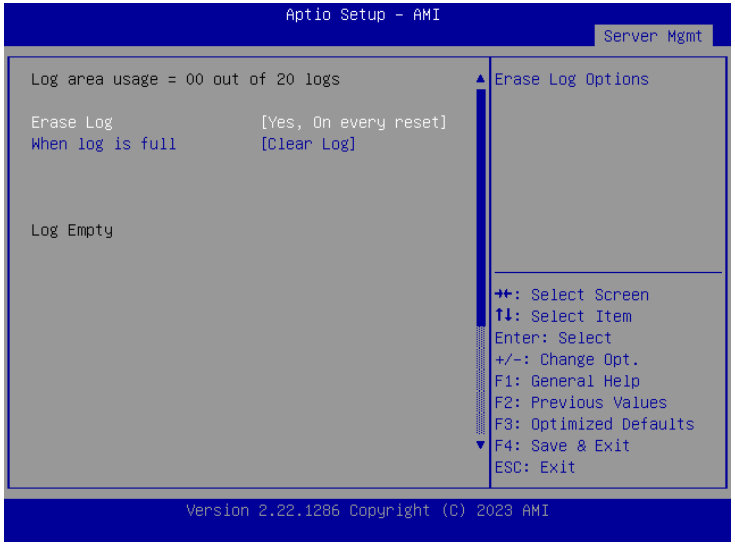
When SEL is Full

Configures the action to perform when SEL is full.

Log EFI Status Codes

Configures the options for logging EFI status codes.

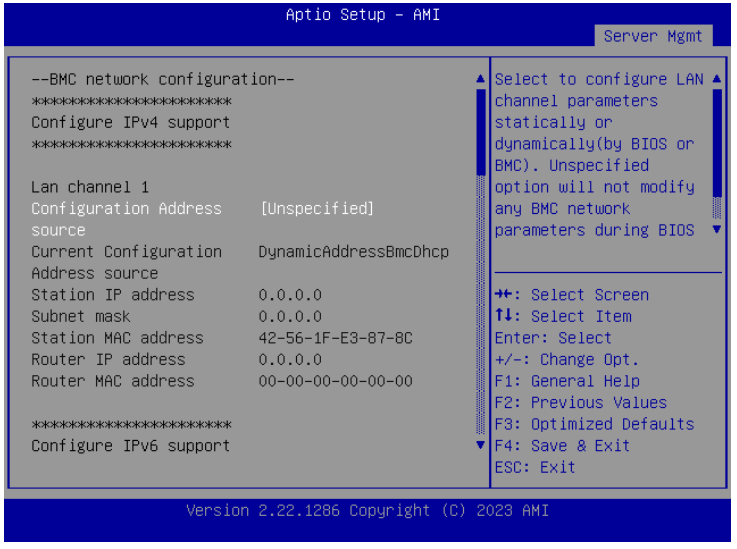
Server Mgmt > Bmc self test log



Erase Log
Configures the options for erasing log.

When SEL is Full
Configures the action to perform when SEL is full.

Server Mgmt > BMC network configuration

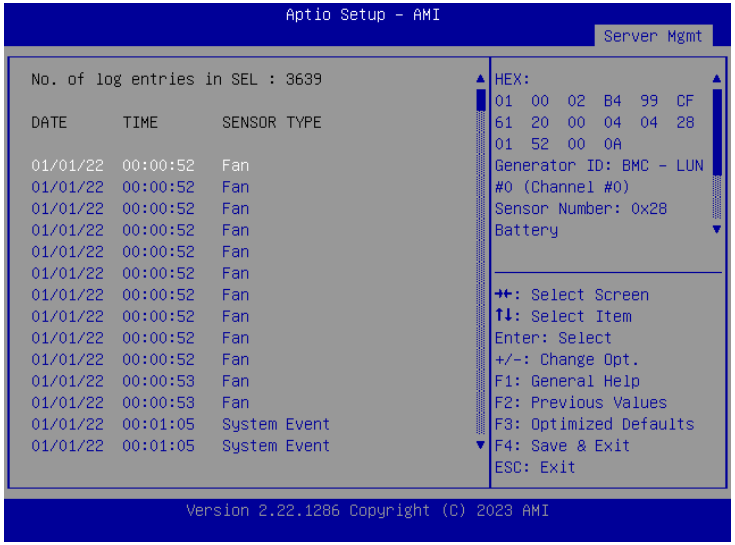


Configuration Address source
Selects to configure LAN channel parameters statically or dynamically (by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.

IPv6 Support
Enables or disables IPv6 support for LAN channel 1.

VLAN Support
Enables VLAN support to specify the 802.1q VLAN ID.

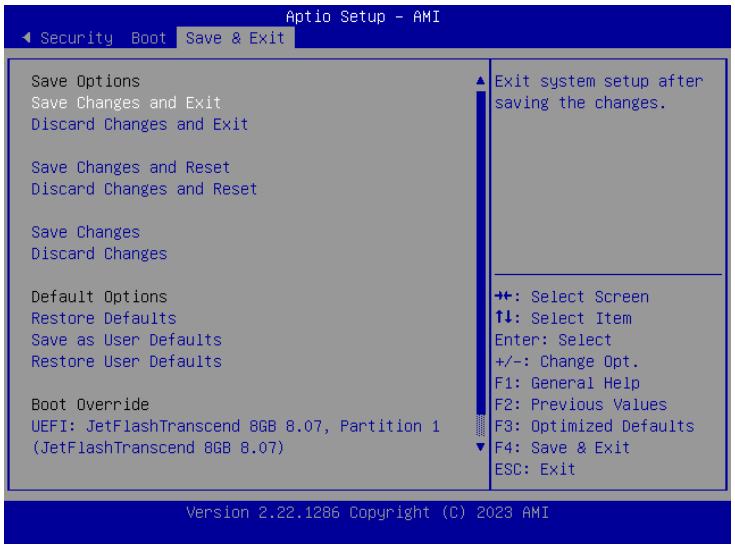
Server Mgmt > View System Event Log



View System Event Log

Displays system event log information including date, time, and sensor type.

Save & Exit



Save Changes and Exit
To save the changes and exit the Setup utility, select this field then press <Enter>. A dialog box will appear. Confirm by selecting Yes. You can also press <F4> to save and exit Setup.

Discard Changes and Exit
To exit the Setup utility without saving the changes, select this field then press <Enter>. You may be prompted to confirm again before exiting. You can also press <ESC> to exit without saving the changes.

Save Changes and Reset
To save the changes and reset, select this field then press <Enter>. A dialog box will appear. Confirm by selecting Yes.

Discard Changes and Reset
To exit the Setup utility without saving the changes, select this field then press <Enter>. You may be prompted to confirm again before exiting.

Restore Defaults
To restore the BIOS to default settings, select this field then press <Enter>. A dialog box will appear. Confirm by selecting Yes.

Save as User Defaults
To use the current configurations as user default settings for the BIOS, select this field then press <Enter>. A dialog box will appear. Confirm by selecting Yes.

Restore User Defaults
To restore the BIOS to user default settings, select this field then press <Enter>. A dialog box will appear. Confirm by selecting Yes.

Boot Override
To bypass the boot sequence from the Boot Option List and boot from a particular device, select the desired device and press <Enter>.