NEXCOM International Co., Ltd.

Network and Communication Solutions

Network Security Appliance

NSA 7150/7150A

User Manual

NEXCOM International Co., Ltd.
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PREFACE

Copyright

Disclaimer

The information in this document is subject to change without prior notice and does not represent commitment from NEXCOM International Co., Ltd. However, users may update their knowledge of any product in use by constantly checking its manual posted on our website: http://www.nexcom.com. NEXCOM shall not be liable for direct, indirect, special, incidental, or consequential damages arising out of the use of any product, nor for any infringements upon the rights of third parties, which may result from such use. Any implied warranties of merchantability or fitness for any particular purpose is also disclaimed.

Acknowledgements

NSA 7150 and NSA 7150A are trademarks of NEXCOM International Co., Ltd. All other product names mentioned herein are registered trademarks of their respective owners.

Regulatory Compliance Statements

This section provides the FCC compliance statement for Class A devices and describes how to keep the system CE compliant.

Declaration of Conformity

FCC

This equipment has been tested and verified to comply with the limits for a Class A digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area (domestic environment) is likely to cause harmful interference, in which case the user will be required to correct the interference (take adequate measures) at their own expense.

CE

The product(s) described in this manual complies with all applicable European Union (CE) directives if it has a CE marking. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cable and cabling techniques.

RoHS Compliance

NEXCOM RoHS Environmental Policy and Status Update

NEXCOM is a global citizen for building the digital infrastructure. We are committed to providing green products and services, which are compliant with European Union RoHS (Restriction on Use of Hazardous Substance in Electronic Equipment) directive 2011/65/EU, to be your trusted green partner and to protect our environment.

RoHS restricts the use of Lead (Pb) < 0.1% or 1,000ppm, Mercury (Hg) < 0.1% or 1,000ppm, Cadmium (Cd) < 0.01% or 100ppm, Hexavalent Chromium (Cr6+) < 0.1% or 1,000ppm, Polybrominated biphenyls (PBB) < 0.1% or 1,000ppm, and Polybrominated diphenyl Ethers (PBDE) < 0.1% or 1,000ppm.

In order to meet the RoHS compliant directives, NEXCOM has established an engineering and manufacturing task force in to implement the introduction of green products. The task force will ensure that we follow the standard NEXCOM development procedure and that all the new RoHS components and new manufacturing processes maintain the highest industry quality levels for which NEXCOM are renowned.

The model selection criteria will be based on market demand. Vendors and suppliers will ensure that all designed components will be RoHS compliant.

How to recognize NEXCOM RoHS Products?

For existing products where there are non-RoHS and RoHS versions, the suffix "(LF)" will be added to the compliant product name.

All new product models launched after January 2013 will be RoHS compliant. They will use the usual NEXCOM naming convention.

Warranty and RMA

NEXCOM Warranty Period

NEXCOM manufactures products that are new or equivalent to new in accordance with industry standard. NEXCOM warrants that products will be free from defect in material and workmanship for 2 years, beginning on the date of invoice by NEXCOM.

NEXCOM Return Merchandise Authorization (RMA)

- Customers shall enclose the "NEXCOM RMA Service Form" with the returned packages.
- Customers must collect all the information about the problems encountered and note anything abnormal or, print out any on-screen messages, and describe the problems on the "NEXCOM RMA Service Form" for the RMA number apply process.
- Customers can send back the faulty products with or without accessories (manuals, cable, etc.) and any components from the card, such as CPU and RAM. If the components were suspected as part of the problems, please note clearly which components are included. Otherwise, NEXCOM is not responsible for the devices/parts.
- Customers are responsible for the safe packaging of defective products, making sure it is durable enough to be resistant against further damage and deterioration during transportation. In case of damages occurred during transportation, the repair is treated as "Out of Warranty."
- Any products returned by NEXCOM to other locations besides the customers' site will bear an extra charge and will be billed to the customer.

Repair Service Charges for Out-of-Warranty Products

NEXCOM will charge for out-of-warranty products in two categories, one is basic diagnostic fee and another is component (product) fee.

System Level

- Component fee: NEXCOM will only charge for main components such as SMD chip, BGA chip, etc. Passive components will be repaired for free, ex: resistor, capacitor.
- Items will be replaced with NEXCOM products if the original one cannot be repaired. Ex: motherboard, power supply, etc.
- Replace with 3rd party products if needed.
- If RMA goods can not be repaired, NEXCOM will return it to the customer without any charge.

Board Level

- Component fee: NEXCOM will only charge for main components, such as SMD chip, BGA chip, etc. Passive components will be repaired for free, ex: resistors, capacitors.
- If RMA goods can not be repaired, NEXCOM will return it to the customer without any charge.

Warnings

Read and adhere to all warnings, cautions, and notices in this guide and the documentation supplied with the chassis, power supply, and accessory modules. If the instructions for the chassis and power supply are inconsistent with these instructions or the instructions for accessory modules, contact the supplier to find out how you can ensure that your computer meets safety and regulatory requirements.

Cautions

Electrostatic discharge (ESD) can damage system components. Do the described procedures only at an ESD workstation. If no such station is available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the computer chassis.

Safety Information

Before installing and using the device, note the following precautions:

- Read all instructions carefully.
- Do not place the unit on an unstable surface, cart, or stand.
- Follow all warnings and cautions in this manual.
- When replacing parts, ensure that your service technician uses parts specified by the manufacturer.
- Avoid using the system near water, in direct sunlight, or near a heating device.
- The load of the system unit does not solely rely for support from the rackmounts located on the sides. Firm support from the bottom is highly necessary in order to provide balance stability.
- The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Installation Recommendations

Ensure you have a stable, clean working environment. Dust and dirt can get into components and cause a malfunction. Use containers to keep small components separated.

Adequate lighting and proper tools can prevent you from accidentally damaging the internal components. Most of the procedures that follow require only a few simple tools, including the following:

- A Philips screwdriver
- A flat-tipped screwdriver
- A grounding strap
- An anti-static pad

Using your fingers can disconnect most of the connections. It is recommended that you do not use needle-nose pliers to disconnect connections as these can damage the soft metal or plastic parts of the connectors.

Safety Precautions

1. Read these safety instructions carefully.

2. Keep this User Manual for later reference.

3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.

4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.

5. Keep this equipment away from humidity.

6. Put this equipment on a stable surface during installation. Dropping it or letting it fall may cause damage.

7. The openings on the enclosure are for air convection to protect the equipment from overheating. DO NOT COVER THE OPENINGS.

8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.

9. Place the power cord in a way so that people will not step on it. Do not place anything on top of the power cord. Use a power cord that has been approved for use with the product and that it matches the voltage and current marked on the product's electrical range label. The voltage and current rating of the cord must be greater than the voltage and current rating marked on the product.

10. All cautions and warnings on the equipment should be noted.

11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.

12. Never pour any liquid into an opening. This may cause fire or electrical shock.

13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.

14. If one of the following situations arises, get the equipment checked by service personnel:
    a. The power cord or plug is damaged.
    b. Liquid has penetrated into the equipment.
    c. The equipment has been exposed to moisture.
    d. The equipment does not work well, or you cannot get it to work according to the user's manual.
    e. The equipment has been dropped and damaged.
    f. The equipment has obvious signs of breakage.

15. Do not place heavy objects on the equipment.

16. The unit uses a three-wire ground cable which is equipped with a third pin to ground the unit and prevent electric shock. Do not defeat the purpose of this pin. If your outlet does not support this kind of plug, contact your electrician to replace your obsolete outlet.

17. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER. DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

Technical Support and Assistance

1. For the most updated information of NEXCOM products, visit NEXCOM's website at www.nexcom.com.

2. For technical issues that require contacting our technical support team or sales representative, please have the following information ready before calling:
   - Product name and serial number
   - Detailed information of the peripheral devices
   - Detailed information of the installed software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wordings of the error messages

Warning!

1. Handling the unit: carry the unit with both hands and handle it with care.

2. Maintenance: to keep the unit clean, use only approved cleaning products or clean with a dry cloth.

Conventions Used in this Manual

Warning:
Information about certain situations, which if not observed, can cause personal injury. This will prevent injury to yourself when performing a task.

Caution:
Information to avoid damaging components or losing data.

Note:
Provides additional information to complete a task easily.

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Package Contents

Before continuing, verify that the NSA 7150/7150A package that you received is complete. Your package should have all the items listed in the following table.

Item	Part Number	Name	Qty
1	19S00715000X0	NSA 7150	1
2	50311F0110X00	Flat Head Screw	8
3	5044440031X00	Rubber Foot Set	4
4	6023309081X00	DB9-to-RJ45 Console Cable	1
5	5050300975X00	NSA 7150 Series Heat Sink	2
6	5061600239H00	CPU Socket Carrier	2
7	50311F0654X00	I Head Screw	1
8	50311F0162X00	Round Head Screw	1
9	5040150001X00	Hook Handle (For retrieving LAN module)	1
10	5040290005X00	Ear Set	1

Ordering Information

The following information below provides ordering information for NSA 7150/7150A.

Barebone

NSA 7150 (P/N: 10S00715000X0)

2U, dual Intel® 3rd Xeon® Scalable Processor, w/o QAT, LCM, 8 x LAN modules and RunBMC

NSA 7150A (P/N: 10S00715001X0)

2U, dual Intel® 3rd Xeon® Scalable Processor, w/ QAT, LCM, 8 x LAN modules and RunBMC

LAN Modules

Model	P/N	Interface	Type	Port Number	Bypass/ Segment	Expansion Slot	Speed	Location Slot
NI 184CX1W	2BS10184C04X0	i350AM4x2	PCIe x8	8 Copper	4 bypass	None	1G	3,4/7,8
NI 180CW	2BS10180C02X0	i350AM4x2	PCIe x8	8 Copper	None	None	1G	3,4/7,8
NI 142CX1W	2BS10142C02X0	i350AM4x1	PCIe x8	4 Copper	2 bypass	None	1G	3,4/7,8
NI 140C-OS	2BS10140C00X0	i350AM4x1	PCIe x8	4 Copper	None	None	1G	1,2/5,6
NI 142CX1-OS	2BS10142C00X0	i350AM4x1	PCIe x8	4 Copper	2 bypass	None	1G	1,2/5,6
NI 180C-OS	2BS10180C00X0	i350AM4x2	PCIe x8	8 Copper	None	None	1G	1,2/5,6
NI 184CX1-OS	2BS10184C02X0	i350AM4x2	PCIe x8	8 Copper	4 bypass	None	1G	1,2/5,6
NX 120F-OS	2BS20120F00X0	XL710-BM2	PCIe x8	2 SFP+	None	None	10G	1,2/5,6
NX 140FW	2BS20140F06X0	XL710-BM1	PCIe x8	4 SFP+	None	None	10G	3,4/7,8
NX 140F-OS	2BS20140F02X0	XL710-BM1	PCIe x8	4 SFP+	None	None	10G	1,2/5,6
NX 140C2F2W	2BS20140F07X0	EZX710TM4	PCIe x8	2 Copper+ 2 SFP+	None	None	10G	3,4/7,8
NX 142FX1W	2BS20142F05X0	XL710-BM1	PCIe x8	4 SFP+	2 bypass	None	10G	3,4/7,8
NX 142FX1W-LR	2BS20142F06X0	XL710-BM1	PCIe x8	4 SFP+	2 bypass	None	10G	3,4/7,8
NX 142FX1-OS	2BS20142F01X0	XL710-BM1	PCIe x8	4 SFP+	2 bypass	None	10G	1,2/5,6
NX 142FX1-LR-OS	2BS20142F02X0	XL710-BM1	PCIe x8	4 SFP+	2 bypass	None	10G	1,2/5,6
NX 121FX1-OS	2BS20121F02X0	XL710-BM2	PCIe x8	2 SFP+	1 bypass	None	10G	1,2/5,6
NX 121FX1-LR-OS	2BS20121F03X0	XL710-BM2	PCIe x8	2 SFP+	1 bypass	None	10G	1,2/5,6
NV 120FW	2BS50120F01X0	XXV710-AM2	PCIe x8	2 SPF28	None	None	25G	3,4/7,8
NQ 120FW	2BS40120F01X0	XL710-BM2	PCIe x8	2 QSFP+	None	None	40G	3,4/7,8
NC 120FMS4W	2BS30012002X0	MT28808A0-FCCF-EV	PCIe x8	2 QSFP28	None	None	100G	3,4/7,8
NC 120FIS4-OS	2BS30012001X0	EZE810CAM2	PCIe x16	2 QSFP28	None	None	100G	1,2/5,6
NL 110FM-OS	2BS60011000X0	MT28924A0-NCCF-VE	PCIe x16	1 QSFP28/56	None	None	200G	1,2/5,6

Chapter 1: Product Introduction

Overview

Key Features

- 3rd generation dual Intel® Xeon® scalable processor
- 20 x DDR4 3200 ECC RDIMM/LRDIMM
- Support Intel® Optane™ Persistent Memory
- 2 x 2.5” swappable SSD/HDDs
- 2 x Management ports
- 8 x PCIe 4 LAN modules
- Support Intel® QAT (NSA7150A)
- 1 x PCIe 4 x16 low profile riser card
- 1 x PCIe 4 x16 FHFL card (Optional)
- Support OCP NIC 3.0
- Support IPMI 2.0 RunBMC
- 1300W 1+1 CRPS redundant power supply

Hardware Specifications

Main Board

- 3rd generation dual Intel® Xeon® scalable processor family
- Support 3 x UPI between CPUs
- Intel® C627A w/ Intel® QAT (NSA7150A)
- Support IPMI 2.0 RunBMC (optional)
- Support 8 x PCIe 4 LAN modules

PCH

NSA 7150: Intel® Lewisburg Refresh LBG-1G (C621A)
NSA 7150A: Intel® Lewisburg Refresh LBG-T (C627A)

Main Memory

- Support 20 (10+10) DDR4 memory DIMMs
  (Maximum 1280GB for RDIMM and 2560GB for LRDIMM)
- Support Intel Optane™ Persistent Memory (Barlow Pass)

Storage

- 2 x 2.5" swappable SSD/HDDs
- 1 x M.2 2280 (M Key) socket

I/O Interface-External

- Button: Power & Reset & NMI
- LED: PWR/STBY/HDD/ERR
- 2 x 2.5" swappable SSD/HDD bays
- 2 x USB 3.0 ports
- 1 x RJ45 type console
- 8 x LAN Module Slots + 1 x PCIe 4 x16 Low Profile Card
- 8 x OCP NIC 3.0 Slots + 1 x PCIe 4 x16 Low Profile Card (Optional)
- 4 x LAN Module Slots + 1 x PCIe 4 x16 FHFL Card (Optional)
- 2 x Management ports
- 1 x VGA port (for BMC SKU)
- 3 x Swappable smart fans
- 2 x Power inlets
- LCM module

I/O Interface-Internal

- TPM 2.0 module (optional)
- RunBMC module (optional)

Power Input

- 1300W 1+1 CRPS redundant power supply

Dimensions and Weight

- Chassis dimension: 438 mm x 650 mm x 88 mm
- Carton dimension: 774 mm x 636 mm x 293 mm
- Without packing: TBD
- With packing: TBD

Environment

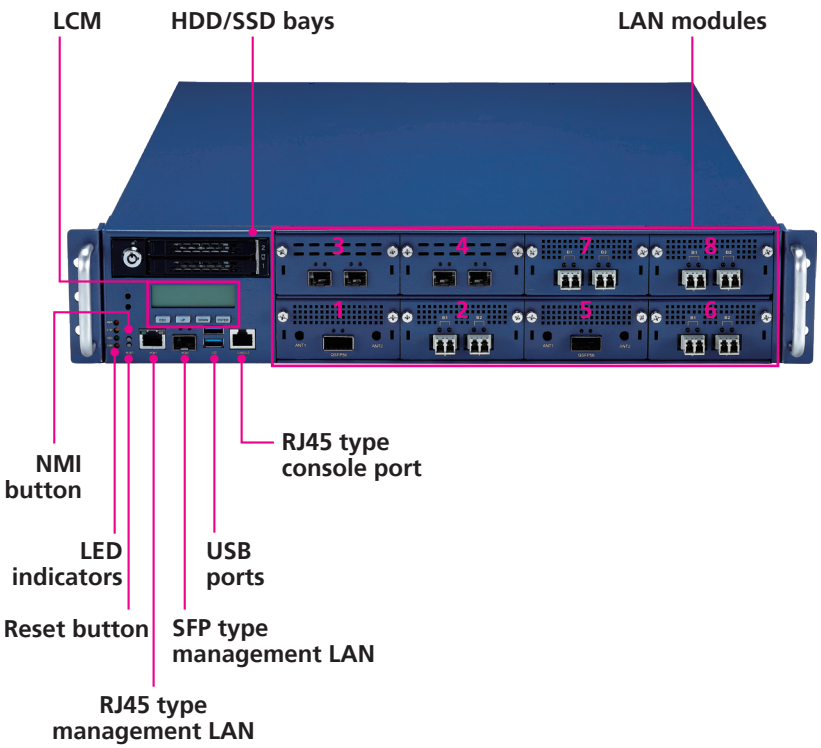
- Operating temperature: 0°C~40°C
- Storage temperature: -20°C~75°C
- Relative humidity: 10%~90% non-condensing

Certifications

- CE approval
- FCC Class A
- UL

Knowing Your NSA 7150

Front Panel



LCM (Liquid Crystal Display Module)
Reserved for the user to define.

NMI Button
Press to issue a Non-Maskable Interrupt (NMI) for debugging purposes.

HDD/SDD Bays
Two 2.5" HDD/SSD swappable bays for installing HDD/SSDs.

LED Indicators
Indicates the power status, error status and storage drive activity of the system.

Reset Button
Press to restart the system.

RJ45 Type Management LAN Port
RJ45 type LAN ports used for managing the system.

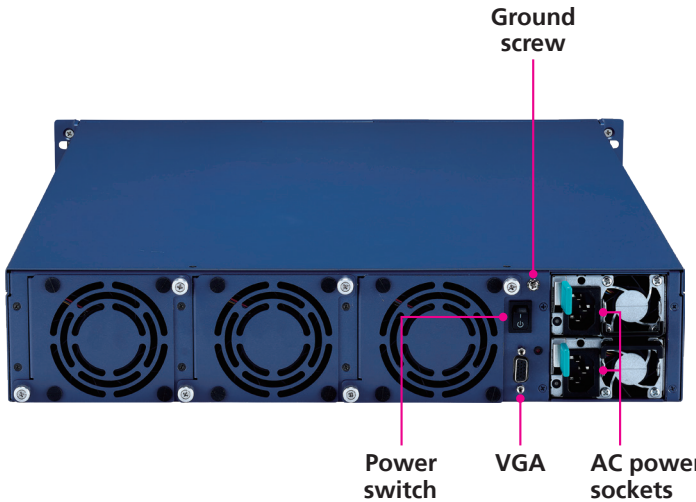
SFP Type Management LAN Port
SFP port used for managing the system.

USB Ports
Used to connect USB 3.0/2.0/1.1 devices.

RJ45 Type Console Serial Port
Used to connect console devices with RJ45 type connection.

LAN Modules
Eight LAN module bays.

Rear Panel



Power Switch
Press to power-on or power-off the system.

VGA
Used to connect an analog VGA monitor.

AC Power Sockets
Dual redundant power supply sockets, plug an AC power cord here before turning on the system.

Ground Screw
The round head screw included in the accessory pack (P/N: 50311F0162X00) can be installed here as the ground screw. Ensure that the ground screw is installed first before use.

Chapter 2: Jumpers and Connectors

This chapter describes how to set the jumpers and connectors on the NSA 7150/7150A motherboard.

Before You Begin

- Ensure you have a stable, clean working environment. Dust and dirt can get into components and cause a malfunction. Use containers to keep small components separated.
- Adequate lighting and proper tools can prevent you from accidentally damaging the internal components. Most of the procedures that follow require only a few simple tools, including the following:
  - A Philips screwdriver
  - A flat-tipped screwdriver
  - A set of jewelers screwdrivers
  - A grounding strap
  - An anti-static pad
- Using your fingers can disconnect most of the connections. It is recommended that you do not use needle-nosed pliers to disconnect connections as these can damage the soft metal or plastic parts of the connectors.
- Before working on internal components, make sure that the power is off. Ground yourself before touching any internal components, by touching a metal object. Static electricity can damage many of the electronic components. Humid environments tend to have less static electricity than dry environments. A grounding strap is warranted whenever danger of static electricity exists.

Precautions

Computer components and electronic circuit boards can be damaged by discharges of static electricity. Working on computers that are still connected to a power supply can be extremely dangerous.

Follow the guidelines below to avoid damage to your computer or yourself:

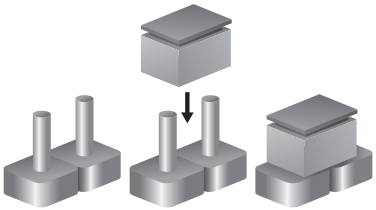
- Always disconnect the unit from the power outlet whenever you are working inside the case.
- If possible, wear a grounded wrist strap when you are working inside the computer case. Alternatively, discharge any static electricity by touching the bare metal chassis of the unit case, or the bare metal body of any other grounded appliance.
- Hold electronic circuit boards by the edges only. Do not touch the components on the board unless it is necessary to do so. Don't flex or stress the circuit board.
- Leave all components inside the static-proof packaging that they shipped with until they are ready for installation.
- Use correct screws and do not over tighten screws.

Jumper Settings

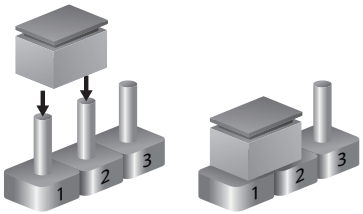
A jumper is the simplest kind of electric switch. It consists of two metal pins and a cap. When setting the jumpers, ensure that the jumper caps are placed on the correct pins. When the jumper cap is placed on both pins, the jumper is short. If you remove the jumper cap, or place the jumper cap on just one pin, the jumper is open.

Refer to the illustrations below for examples of what the 2-pin and 3-pin jumpers look like when they are short (on) and open (off).

Two-Pin Jumpers: Open (Left) and Short (Right)

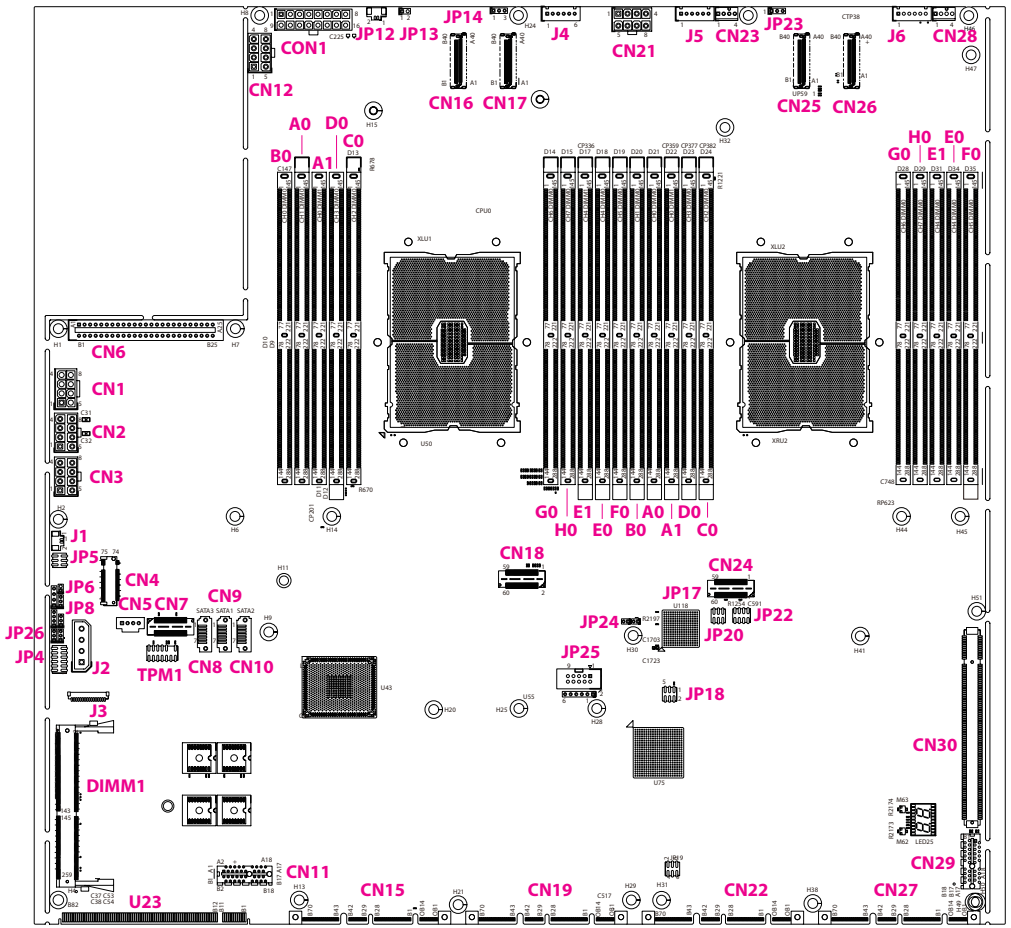


Three-Pin Jumpers: Pins 1 and 2 are Short



Locations of the Jumpers and Connectors

The figure below shows the location of the jumpers and connectors.



Jumper

RTC Clear

Connector type: 1x3 3-pin header
Connector location: JP8

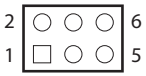
Pin	Function
1-2 On	Normal
2-3 On	Clear CMOS

1-2 On: default

Pin	Definition
1	NC
2	RST_RTCRST_N
3	GND

XDP Debug Header

Connector type: 2x3 6-pin header
Connector location: JP5



Pin	Function
1-3 On	Force Bypass of CPU1
3-5 On	Normal Operation
2-4 On	Force Bypass of CPU2
4-6 On	Normal Operation

3-5, 4-6 On: default

Pin	Definition	Pin	Definition
1	NC	2	NC
3	FM_CPU1_SKTOCC_N	4	FM_CPU2_SKTOCC_N
5	FM_CPU1_SKTOCC_ LVT3_N	6	FM_CPU2_SKTOCC_ LVT3_N

BMC Remote SPD Debug Header

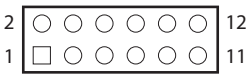
Connector type: 1x2 2-pin header
Connector location: JP6

Pin	Function
1-2 On	SPD Remote Debug Enabled

Pin	Definition
1	P3V3_AUX
2	RST_SMB_SWITCH_N

PCH Strap Debug Use

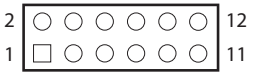
Connector type: 2x6 12-pin header
Connector location: JP4



Pin	Function
1-3 On	ME Force Update
1-3 Off	Normal (Default)
5-7 On	Password Clear
5-7 Off	Normal (Default)
2-4 On	LT Key Downgrade Enable
2-4 Off	LT Key Downgrade Disable (Default)
6-8 On	Flash Security Override Enable
6-8 Off	Flash Security Override Disable (Default)
10-12 On	Top Swap Enable
10-12 Off	Top Swap Disable (Default)

PCH Strap Debug Use

Connector type: 2x6 12-pin header
Connector location: JP4



Pin	Definition	Pin	Definition
1	FM_ME_RCVR_N	2	FM_LT_KEY_ DOWNGRADE_N
3	GND	4	GND
5	FM_PASSWORD_ CLEAR_N	6	P3V3_AUX
7	GND	8	AUD_AZA_SDO
9	FM_PCH_BMC_ THRMTRIP_EXI_STRAP_N	10	P3V3_AUX
11	GND	12	FM_PCH_BIOS_RCVR_ SPKR

CPLD JTAG Select

Connector type: 1x2 2-pin header
Connector location: JP17

Pin	Function
1-2 On	JTAG Header to CPLD JTAG Pin
1-2 Off	BMC to CPLD JTAG Pin (Default)

Pin	Definition
1	JTAG_SEL
2	GND

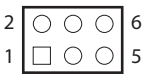
CPLD JTAG Select

Connector type: 1x2 2-pin header
Connector location: JP24

Pin	Function
1-2 On	Flash CPLD from JTAG
1-2 Off	Normal (For remote update CPLD)

PFR Recovery

Connector type: 2x3 6-pin header
Connector location: JP20

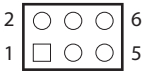


Pin	Function
1-2 On	Force PFR Recovery
1-2 Off	Normal Operation (Default)
3-4 On	Force PFR CPLD Update
3-4 Off	Normal Operation (Default)
5-6 On	PFR CPLD in Debug Mode
5-6 Off	Normal Operation (Default)

Pin	Definition	Pin	Definition
1	FM_PFR_FORCE_ RECOVERY_N	2	GND
3	FM_PFR_PROV_ UPDATE_N	4	GND
5	FM_PFR_DEBUG_ MODE_N	6	GND

AT/ATX Header & CPLD JTAG PROG Enable Header

Connector type: 2x3 6-pin header
Connector location: JP18



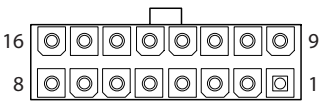
Pin	Function
1-3 On	ATX (Default)
3-5 On	AT
2-4 On	Enable PROG (Default)
4-6 On	Disable PROG

Pin	Definition	Pin	Definition
1	P3V3_CPLD	2	P3V3_CPLD
3	AT_ATX_SEL	4	JTAG_PLD_JTAGEN
5	GND	6	GND

Internal Connectors

Internal Power Connector (CON1 to CN1, CN21)

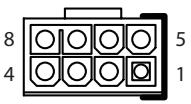
Connector type: 2x8 16-pin header
Connector location: CON1



Pin	Definition	Pin	Definition
1	GND	2	GND
3	GND	4	GND
5	P12V_AUX	6	P12V_AUX
7	P12V	8	P12V
9	P12V_AUX	10	P12V_AUX
11	P12V_AUX	12	P12V_AUX
13	P12V_AUX	14	P12V_AUX
15	P12V	16	P12V

Internal Power Connector (CN1 to CON1)

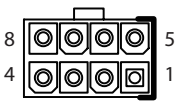
Connector type: 2x4 8-pin header
Connector location: CN1



Pin	Definition	Pin	Definition
1	GND	2	GND
3	GND	4	GND
5	P12V_AUX	6	P12V_AUX
7	P12V_AUX	8	P12V_AUX

Internal Power Connector (CN2 to CN12)

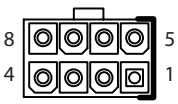
Connector type: 2x4 8-pin header
Connector location: CN2 and CN12



Pin	Definition	Pin	Definition
1	GND	2	GND
3	GND	4	GND
5	P12V	6	P12V
7	P12V	8	P12V

Internal Power Connector

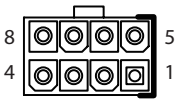
Connector type: 2x4 8-pin header
Connector location: CN3



Pin	Definition	Pin	Definition
1	GND	2	GND
3	GND	4	GND
5	P12V	6	P12V
7	P12V	8	P12V

Internal Power Connector (CON1 to CN21)

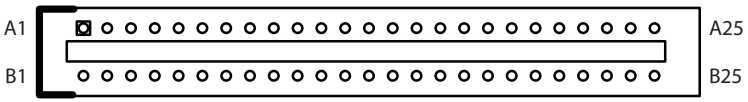
Connector type: 2x4 8-pin header
Connector location: CN21



Pin	Definition	Pin	Definition
1	P12V_AUX	2	P12V_AUX
3	P12V	4	P12V
5	P12V_AUX	6	P12V_AUX
7	P12V	8	P12V

Power Connector to Power Board

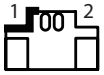
Connector type: 2x25 50-pin header
Connector location: CN6



Pin	Definition	Pin	Definition
A1-9	GND	B1-9	GND
A10-18	P12V	B10-18	P12V
A19	SMB_PFR_PMB1_STBY_LVC3_CRPS_SDA	B19	GND
A20	SMB_PFR_PMB1_STBY_LVC3_CRPS_SCL	B20	FM_PS_EN_PSU_N
A21	GND	B21	P12V_STBY_PSU
A22	IRQ_SML1_PMBUS_BMC_ALERT_N	B22	RETURN_SENSE
A23	PWRGD_PS_PWROK	B23	CRPS_PRESEND1
A24	AC_FAIL_PSU	B24	12V_REMOTE_SENSE
A25	P3V3_CPLD	B25	CRPS_PRESEND2

Header to LED

Connector type: 1x2 2-pin header
Connector location: JP12



Pin	Definition
1	P3V3_CPLD
2	ID_LED_N

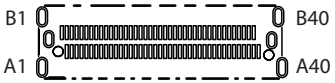
Header to BTN Switch

Connector type: 1x2 2-pin header
Connector location: JP13

Pin	Definition
1	PWRBTN_N
2	GND

OCulink Connector

Connector type: 2x40 80-pin header
Connector location: CN16, CN17 and CN25

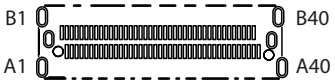


Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE_SLOT_RX_DP0	B2	PE_SLOT_TX_C_DP0
A3	PE_SLOT_RX_DN0	B3	PE_SLOT_TX_C_DN0
A4	GND	B4	GND
A5	PE_SLOT_RX_DP1	B5	PE_SLOT_TX_C_DP1
A6	PE_SLOT_RX_DN1	B6	PE_SLOT_TX_C_DN1
A7	GND	B7	GND
A8	SLOT_R2_SCL	B8	PE_SLOT_PWRBRK0#
A9	SLOT_R2_SDA	B9	IRQ_LVC3_WAKE_SLOT_N
A10	NC	B10	NC
A11	PE_SLOT_RST_N	B11	NC
A12	NC	B12	NC
A13	GND	B13	GND
A14	PE_SLOT_RX_DP2	B14	PE_SLOT_TX_C_DP2
A15	PE_SLOT_RX_DN2	B15	PE_SLOT_TX_C_DN2
A16	GND	B16	GND
A17	PE_SLOT_RX_DP3	B17	PE_SLOT_TX_C_DP3
A18	PE_SLOT_RX_DN3	B18	PE_SLOT_TX_C_DN3
A19	GND	B19	GND
A20	NC	B20	NC

Pin	Definition	Pin	Definition
A21	NC	B21	NC
A22	GND	B22	GND
A23	PE_SLOT_RX_DP4	B23	PE_SLOT_TX_C_DP4
A24	PE_SLOT_RX_DN4	B24	PE_SLOT_TX_C_DN4
A25	GND	B25	GND
A26	PE_SLOT_RX_DP5	B26	PE_SLOT_TX_C_DP5
A27	PE_SLOT_RX_DN5	B27	PE_SLOT_TX_C_DN5
A28	GND	B28	GND
A29	NC	B29	NC
A30	NC	B30	NC
A31	NC	B31	NC
A32	NC	B32	NC
A33	NC	B33	NC
A34	GND	B34	GND
A35	PE_SLOT_RX_DP6	B35	PE_SLOT_TX_C_DP6
A36	PE_SLOT_RX_DN6	B36	PE_SLOT_TX_C_DN6
A37	GND	B37	GND
A38	PE_SLOT_RX_DP7	B38	PE_SLOT_TX_C_DP7
A39	PE_SLOT_RX_DN7	B39	PE_SLOT_TX_C_DN7
A40	GND	B40	GND

OCulink Connector

Connector type: 2x40 80-pin header
Connector location: CN26



Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE_SLOT_RX_DP0	B2	PE_SLOT_TX_C_DP0
A3	PE_SLOT_RX_DN0	B3	PE_SLOT_TX_C_DN0
A4	GND	B4	GND
A5	PE_SLOT_RX_DP1	B5	PE_SLOT_TX_C_DP1
A6	PE_SLOT_RX_DN1	B6	PE_SLOT_TX_C_DN1
A7	GND	B7	GND
A8	NC	B8	NC
A9	NC	B9	NC
A10	NC	B10	NC
A11	NC	B11	NC
A12	NC	B12	NC
A13	GND	B13	GND
A14	PE_SLOT_RX_DP2	B14	PE_SLOT_TX_C_DP2
A15	PE_SLOT_RX_DN2	B15	PE_SLOT_TX_C_DN2
A16	GND	B16	GND
A17	PE_SLOT_RX_DP3	B17	PE_SLOT_TX_C_DP3
A18	PE_SLOT_RX_DN3	B18	PE_SLOT_TX_C_DN3
A19	GND	B19	GND
A20	NC	B20	NC

Pin	Definition	Pin	Definition
A21	NC	B21	NC
A22	GND	B22	GND
A23	PE_SLOT_RX_DP4	B23	PE_SLOT_TX_C_DP4
A24	PE_SLOT_RX_DN4	B24	PE_SLOT_TX_C_DN4
A25	GND	B25	GND
A26	PE_SLOT_RX_DP5	B26	PE_SLOT_TX_C_DP5
A27	PE_SLOT_RX_DN5	B27	PE_SLOT_TX_C_DN5
A28	GND	B28	GND
A29	NC	B29	NC
A30	NC	B30	NC
A31	NC	B31	NC
A32	NC	B32	NC
A33	NC	B33	NC
A34	GND	B34	GND
A35	PE_SLOT_RX_DP6	B35	PE_SLOT_TX_C_DP6
A36	PE_SLOT_RX_DN6	B36	PE_SLOT_TX_C_DN6
A37	GND	B37	GND
A38	PE_SLOT_RX_DP7	B38	PE_SLOT_TX_C_DP7
A39	PE_SLOT_RX_DN7	B39	PE_SLOT_TX_C_DN7
A40	GND	B40	GND

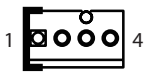
Fan Connector

Connector type: 1x6 6-pin header
Connector location: J4, J5 and J6

Pin	Definition	Pin	Definition
1	GND	2	GND
3	P12V	4	P12V
5	TACH	6	PWM

Fan Connector

Connector type: 1x4 4-pin header
Connector location: CN23 and CN28



Pin	Definition	Pin	Definition
1	GND	2	P12V
3	TACH	4	PWM

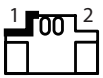
Power Team Debug Header

Connector type: 1x3 3-pin header
Connector location: JP14 (CPU1) and JP23 (CPU2)

Pin	Definition
1	SDA
2	SCL
3	GND

SYS RTC Header

Connector type: 1x2 2-pin header
Connector location: J1



Pin	Definition
1	GND
2	3V3_BAT

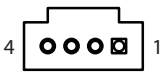
SATA Power Connector

Connector type: 1x4 4-pin header
Connector location: J2

Pin	Definition	Pin	Definition
1	P5V	2	GND
3	GND	4	P12V

IPMB Debug Header Use

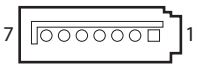
Connector type: 1x4 4-pin header
Connector location: CN5



Pin	Definition	Pin	Definition
1	IPMB_DATA	2	GND
3	IPMB_CLK	4	P5V_AUX

SATA Connectors

Connector type: Standard Serial ATA 7P (1.27mm, SATA-M-180)
Connector location: CN8, CN9 and CN10



Pin	Definition	Pin	Definition
1	GND	2	TXP
3	TXN	4	GND
5	RXN	6	RXP
7	GND		

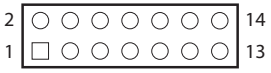
BMC Debug Header

Connector type: 1x4 4-pin header
Connector location: JP26

Pin	Definition	Pin	Definition
1	3.3V	2	UART_RX
3	UART_TX	4	GND

TPM Header

Connector type: 2x7 14-pin header
Connector location: TPM1



Pin	Definition	Pin	Definition
1	P3V3_AUX	2	SPI_PCH_TPM_CS_R_N
3	NC	4	IRQ_TPM_SPI_N
5	RST_PLTRST_TPM_R_N	6	NC
7	NC	8	GND
9	NC	10	SPI_TPM_CLK_R
11	SPI_PCH_MUXED_R_IO1	12	SPI_PCH_MUXED_R_IO0
13	NC	14	NC

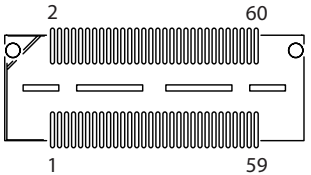
CPLD JTAG for Programming CPLD Code

Connector type: 1x6 6-pin header
Connector location: JP25

Pin	Definition	Pin	Definition
1	P3V3_CPLD	2	GND
3	JTAG_TCK_CPLD	4	JTAG_TDO_CPLD
5	JTAG_TDI_CPLD	6	JTAG_TMS_CPLD

XDP Debug Connector (For PCH)

Connector type: 2x30 60-pin header
Connector location: CN7

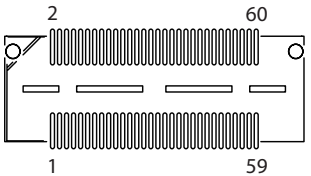


Pin	Definition	Pin	Definition
1	NC	2	NC
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	NC	12	P1V05_PCH_AUX
13	TRC_2CH0_CLK	14	GND
15	GND	16	GND
17	GND	18	NC
19	TRC_2CH0_D0	20	NC
21	TRC_2CH0_D1	22	NC
23	TRC_2CH0_D2	24	NC
25	TRC_2CH0_D3	26	NC
27	TRC_2CH0_D4	28	NC
29	TRC_2CH0_D5	30	NC

Pin	Definition	Pin	Definition
31	TRC_2CH0_D6	32	NC
33	TRC_2CH0_D7	34	NC
35	TRC_2CH1_D0	36	NC
37	TRC_2CH1_D1	38	NC
39	TRC_2CH1_D2	40	NC
41	TRC_2CH1_D3	42	DBP_VISA_RSMRST_N
43	TRC_2CH1_D4	44	NC
45	TRC_2CH1_D5	46	NC
47	TRC_2CH1_D6	48	NC
49	TRC_2CH1_D7	50	NC
51	NC	52	P3V3_AUX
53	NC	54	NC
55	NC	56	NC
57	GND	58	GND
59	TRC_2CH1_CLK	60	GND

XDP Debug Connector (For CPU1)

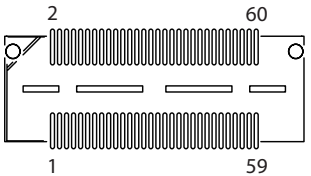
Connector type: 2x30 60-pin header
Connector location: CN18



Pin	Definition	Pin	Definition
1	P1V05_PCH_AUX	2	JTAG_DBP_TMS_R
3	JTAG_DBP_CPU_GTL_TCK_MIPI60_R	4	JTAG_DBP_TDO_R
5	JTAG_DBP_TDI_R	6	RST_DBP_RST_CO_N
7	DBP_ITPMODE_CPUPWRGD	8	PD_TRST_PD3
9	JTAG_DBP_TRST_N	10	H_DBP_PREQ_N_R
11	H_DBP_PRDY_R_N	12	PVCCIO_CPU1
13	MCI_CPU1_PTI0_CLK	14	GND
15	DBP_SPI_PCH_IO2_DEBUG_CONSENT_N	16	GND
17	FM_DBP_PRESENT_R_N	18	GND
19	MCI_CPU1_PTI0	20	GND
21	MCI_CPU1_PTI1	22	GND
23	MCI_CPU1_PTI2	24	GND
25	MCI_CPU1_PTI3	26	GND
27	MCI_CPU1_PTI4	28	GND
29	MCI_CPU1_PTI5	30	GND
31	MCI_CPU1_PTI6	32	GND
33	MCI_CPU1_PTI7	34	NC
35	MCI_CPU1_PTI8	36	DBP_SYSPWROK
37	MCI_CPU1_PTI9	38	FM_CPU_PWR_DEBUG_N
39	MCI_CPU1_PTI10	40	DBP_POWER_BTN_N
41	MCI_CPU1_PTI11	42	RST_DBP_RSMRST_N
43	MCI_CPU1_PTI12	44	NC
45	MCI_CPU1_PTI13	46	NC
47	MCI_CPU1_PTI14	48	SMB_HOST_XDP_STBY_LVC3_SCL
49	MCI_CPU1_PTI15	50	SMB_HOST_XDP_STBY_LVC3_SDA
51	JTAG_DBP_PCH_TCK	52	P3V3_AUX
53	DBP_CPU_OBSFN_B_MBP3_GTL_N	54	NC
55	DBP_HOOK8_MBP2_BOOT_HALT_N	56	NC
57	GND	58	GND
59	MCI_CPU1_PTI1_CLK	60	GND

XDP Debug Connector (For CPU2)

Connector type: 2x30 60-pin header
Connector location: CN24

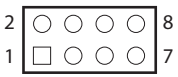


Pin	Definition	Pin	Definition
1	NC	2	NC
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	NC	12	PVCCIO_CPU2
13	MCI_CPU2_PTI0_CLK	14	GND
15	GND	16	GND
17	GND	18	NC
19	MCI_CPU2_PTI0	20	NC
21	MCI_CPU2_PTI1	22	NC
23	MCI_CPU2_PTI2	24	NC
25	MCI_CPU2_PTI3	26	NC
27	MCI_CPU2_PTI4	28	NC
29	MCI_CPU2_PTI5	30	NC

Pin	Definition	Pin	Definition
31	MCI_CPU2_PTI6	32	NC
33	MCI_CPU2_PTI7	34	NC
35	MCI_CPU2_PTI8	36	NC
37	MCI_CPU2_PTI9	38	NC
39	MCI_CPU2_PTI10	40	NC
41	MCI_CPU2_PTI11	42	PWRGD_CPU2_LVC3_ MIPI60
43	MCI_CPU2_PTI12	44	NC
45	MCI_CPU2_PTI13	46	NC
47	MCI_CPU2_PTI14	48	NC
49	MCI_CPU2_PTI15	50	NC
51	NC	52	P3V3_AUX
53	NC	54	NC
55	NC	56	NC
57	GND	58	GND
59	MCI_CPU2_PTI1_CLK	60	GND

GPIO Header

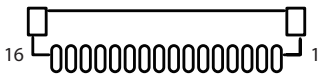
Connector type: 2x4 8-pin header
Connector location: JP22



Pin	Definition	Pin	Definition
1	P3V3_CPLD	2	GND
3	CPLD_GPI01	4	CPLD_GPO01
5	CPLD_GPI02	6	CPLD_GPO02
7	CPLD_GPI03	8	CPLD_GPO03

VGA Connector

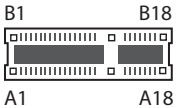
Connector type: 1x16 16-pin header
Connector location: J3



Pin	Definition	Pin	Definition
1	VGA_VCC	2	GND
3	N/C	4	SMB_BMC_DDC_SCL_R1
5	SMB_BMC_DDC_SDA_R1	6	N/C
7	V_BMC_GFX_REAR_ VSYN_R3	8	GND
9	V_BMC_GFX_REAR_ HSYN_R3	10	NC
11	GND	12	V_BMC_GFX_REAR_ BLU_R1
13	GND	14	V_BMC_GFX_REAR_ GRN_R1
15	GND	16	V_BMC_GFX_REAR_ RED_R1

Riser Left Connector

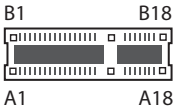
Connector type: PCIe x1
Connector location: CN11



Pin	Definition	Pin	Definition
A1	P12V	B1	P12V
A2	P12V	B2	P12V
A3	P12V	B3	P12V
A4	GND	B4	GND
A5	P3V3	B5	P3V3
A6	P3V3	B6	P3V3
A7	P3V3	B7	P3V3
A8	P3V3	B8	P3V3
A9	P3V3_AUX	B9	P3V3_AUX
A10	GND	B10	GND
A11	GND	B11	GND
A12	GND	B12	GND
A13	PE_SLOT3_CLK_DP	B13	GND
A14	PE_SLOT3_CLK_DN	B14	GND
A15	GND	B15	GND
A16	PE_SLOT4_CLK_DP	B16	GND
A17	PE_SLOT4_CLK_DN	B17	GND
A18	GND	B18	GND

Riser Right Connector

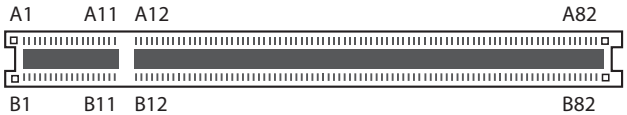
Connector type: PCIe x1
Connector location: CN29



Pin	Definition	Pin	Definition
A1	P12V	B1	P12V
A2	P12V	B2	P12V
A3	P12V	B3	P12V
A4	GND	B4	GND
A5	P3V3	B5	P3V3
A6	P3V3	B6	P3V3
A7	P3V3	B7	P3V3
A8	P3V3	B8	P3V3
A9	P3V3_AUX	B9	P3V3_AUX
A10	GND	B10	GND
A11	GND	B11	GND
A12	GND	B12	GND
A13	PE_SLOT7_CLK_DP	B13	GND
A14	PE_SLOT7_CLK_DN	B14	GND
A15	GND	B15	GND
A16	PE_SLOT8_CLK_DP	B16	GND
A17	PE_SLOT8_CLK_DN	B17	GND
A18	GND	B18	GND

Riser Right Connector

Connector type: PCIe x16
Connector location: CN30



Pin	Definition	Pin	Definition
A1	NC	B1	P12V
A2	P12V	B2	P12V
A3	P12V	B3	P12V
A4	GND	B4	GND
A5	NC	B5	SLOT7_R2_SCL
A6	NC	B6	SLOT7_R2_SDA
A7	NC	B7	GND
A8	NC	B8	P3V3
A9	P3V3	B9	NC
A10	P3V3	B10	P3V3_AUX
A11	PE_SLOT78_RST_N	B11	IRQ_LVC3_WAKE_SLOT78_N
A12	GND	B12	NC
A13	PE_EXPANSION_CLK_DP	B13	GND
A14	PE_EXPANSION_CLK_DN	B14	PE_SLOT8_TX_C_DN7
A15	GND	B15	PE_SLOT8_TX_C_DP7
A16	PE_SLOT8_RX_DN7	B16	GND
A17	PE_SLOT8_RX_DP7	B17	NC
A18	GND	B18	GND

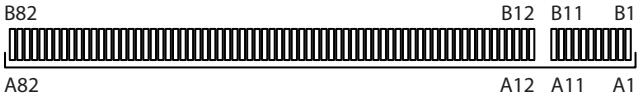
Pin	Definition	Pin	Definition
A19	NC	B19	PE_SLOT8_TX_C_DN6
A20	GND	B20	PE_SLOT8_TX_C_DP6
A21	PE_SLOT8_RX_DN6	B21	GND
A22	PE_SLOT8_RX_DP6	B22	GND
A23	GND	B23	PE_SLOT8_TX_C_DN5
A24	GND	B24	PE_SLOT8_TX_C_DP5
A25	PE_SLOT8_RX_DN5	B25	GND
A26	PE_SLOT8_RX_DP5	B26	GND
A27	GND	B27	PE_SLOT8_TX_C_DN4
A28	GND	B28	PE_SLOT8_TX_C_DP4
A29	PE_SLOT8_RX_DN4	B29	GND
A30	PE_SLOT8_RX_DP4	B30	NC
A31	GND	B31	NC
A32	NC	B32	GND
A33	NC	B33	PE_SLOT8_TX_C_DN3
A34	GND	B34	PE_SLOT8_TX_C_DP3
A35	PE_SLOT8_RX_DN3	B35	GND
A36	PE_SLOT8_RX_DP3	B36	GND

Pin	Definition	Pin	Definition
A37	GND	B37	PE_SLOT8_TX_C_DN2
A38	GND	B38	PE_SLOT8_TX_C_DP2
A39	PE_SLOT8_RX_DN2	B39	GND
A40	PE_SLOT8_RX_DP2	B40	GND
A41	GND	B41	PE_SLOT8_TX_C_DN1
A42	GND	B42	PE_SLOT8_TX_C_DP1
A43	PE_SLOT8_RX_DN1	B43	GND
A44	PE_SLOT8_RX_DP1	B44	GND
A45	GND	B45	PE_SLOT8_TX_C_DN0
A46	GND	B46	PE_SLOT8_TX_C_DP0
A47	PE_SLOT8_RX_DN0	B47	GND
A48	PE_SLOT8_RX_DP0	B48	NC
A49	GND	B49	GND
A50	NC	B50	PE_SLOT7_TX_C_DN7
A51	GND	B51	PE_SLOT7_TX_C_DP7
A52	PE_SLOT7_RX_DN7	B52	GND
A53	PE_SLOT7_RX_DP7	B53	GND
A54	GND	B54	PE_SLOT7_TX_C_DN6
A55	GND	B55	PE_SLOT7_TX_C_DP6
A56	PE_SLOT7_RX_DN6	B56	GND
A57	PE_SLOT7_RX_DP6	B57	GND
A58	GND	B58	PE_SLOT7_TX_C_DN5
A59	GND	B59	PE_SLOT7_TX_C_DP5

Pin	Definition	Pin	Definition
A60	PE_SLOT7_RX_DN5	B60	GND
A61	PE_SLOT7_RX_DP5	B61	GND
A62	GND	B62	PE_SLOT7_TX_C_DN4
A63	GND	B63	PE_SLOT7_TX_C_DP4
A64	PE_SLOT7_RX_DN4	B64	GND
A65	PE_SLOT7_RX_DP4	B65	GND
A66	GND	B66	PE_SLOT7_TX_C_DN3
A67	GND	B67	PE_SLOT7_TX_C_DP3
A68	PE_SLOT7_RX_DN3	B68	GND
A69	PE_SLOT7_RX_DP3	B69	GND
A70	GND	B70	PE_SLOT7_TX_C_DN2
A71	GND	B71	PE_SLOT7_TX_C_DP2
A72	PE_SLOT7_RX_DN2	B72	GND
A73	PE_SLOT7_RX_DP2	B73	GND
A74	GND	B74	PE_SLOT7_TX_C_DN1
A75	GND	B75	PE_SLOT7_TX_C_DP1
A76	PE_SLOT7_RX_DN1	B76	GND
A77	PE_SLOT7_RX_DP1	B77	GND
A78	GND	B78	PE_SLOT7_TX_C_DN0
A79	GND	B79	PE_SLOT7_TX_C_DP0
A80	PE_SLOT7_RX_DN0	B80	GND
A81	PE_SLOT7_RX_DP0	B81	NC
A82	GND	B82	NC

IO Slot Connector

Connector type: 2x82 164-pin header
Connector location: U23



Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	USB3_P01_IO_RXN	B2	USB3_P01_IO_TXN
A3	USB3_P01_IO_RXP	B3	USB3_P01_IO_TXP
A4	GND	B4	GND
A5	USB3_P02_IO_RXN	B5	USB3_P02_IO_TXN
A6	USB3_P02_IO_RXP	B6	USB3_P02_IO_TXP
A7	GND	B7	GND
A8	USB2_P01_IO_DN	B8	USB2_P02_IO_DN
A9	USB2_P01_IO_DP	B9	USB2_P02_IO_DP
A10	GND	B10	GND
A11	FM_OC1_USB_N	B11	NC
A12	GND	B12	GND
A13	CLK_100M_I210_LANB_DP	B13	CLK_100M_I210_LANA_DP
A14	CLK_100M_I210_LANB_DN	B14	CLK_100M_I210_LANA_DN
A15	GND	B15	GND
A16	PCIE_RX_LANB_DP	B16	PCIE_TX_LANB_DP
A17	PCIE_RX_LANB_DN	B17	PCIE_TX_LANB_DN
A18	GND	B18	GND

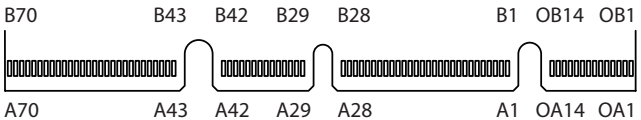
Pin	Definition	Pin	Definition
A19	PCIE_RX_LANA_DP	B19	PCIE_TX_LANA_DP
A20	PCIE_RX_LANA_DN	B20	PCIE_TX_LANA_DN
A21	GND	B21	GND
A22	IRQ_LVC3_WAKE_N	B22	SMB_LANA_CLK_R
A23	GND	B23	SMB_LANA_DATA_R
A24	PE_RST_LAN_N	B24	GND
A25	GND	B25	GND
A26	NCSI_TXD0_A	B26	NCSI_RXD0_A
A27	GND	B27	GND
A28	NCSI_TXD1_A	B28	NCSI_RXD1_A
A29	GND	B29	GND
A30	NCSI_CLK_I210_R1_A	B30	NCSI_CRS_DV_A
A31	GND	B31	GND
A32	NCSI_TX_EN_A	B32	GND
A33	GND	B33	GND
A34	BMC_COM_SW_N	B34	CPLD_UART_DCD_N
A35	IBMC_SIO_LCM_TXD	B35	CPLD_UART_CTS_N
A36	IBMC_SIO_LCM_RXD	B36	CPLD_UART_DSR_N

Pin	Definition	Pin	Definition
A37	GND	B37	CPLD_UART_RI_N
A38	IBMC_SIO_LCM_LED_KR	B38	CPLD_UART_DTR_N
A39	IBMC_SIO_LCM_LED_KG	B39	CPLD_UART_RTS_N
A40	GND	B40	GND
A41	CPLD_UART_R_TXD	B41	BMC_R_TXD5
A42	CPLD_UART_R_RXD	B42	BMC_R_RXD5
A43	GND	B43	GND
A44	GND	B44	GND
A45	GND	B45	GND
A46	GND	B46	GND
A47	GND	B47	GND
A48	GND	B48	GND
A49	GND	B49	GND
A50	GND	B50	GND
A51	GND	B51	GND
A52	GND	B52	GND
A53	GND	B53	GND
A54	GND	B54	GND
A55	GND	B55	GND
A56	GND	B56	GND
A57	GND	B57	LED_PCH_HDD
A58	LED_PWR_STBY_ON	B58	IO_ALERT_LED#
A59	NMI_BTN_N_L	B59	POWER_ERROR_LED

Pin	Definition	Pin	Definition
A60	FP_RST_BTN_N_L	B60	STATUS1_LED
A61	GND	B61	STATUS2_LED
A62	GND	B62	GND
A63	P3V3_CPLD	B63	P3V3_BMC
A64	GND	B64	GND
A65	P3V3	B65	P3V3
A66	P3V3	B66	P3V3
A67	P3V3	B67	P3V3
A68	GND	B68	GND
A69	P3V3_AUX	B69	P3V3_AUX
A70	P3V3_AUX	B70	P3V3_AUX
A71	P3V3_AUX	B71	P3V3_AUX
A72	GND	B72	GND
A73	P5V	B73	P5V
A74	P5V	B74	P5V
A75	GND	B75	GND
A76	P5V_AUX	B76	P5V_AUX
A77	P5V_AUX	B77	P5V_AUX
A78	P5V_AUX	B78	P5V_AUX
A79	GND	B79	GND
A80	GND	B80	GND
A81	GND	B81	GND
A82	GND	B82	GND

OCP Slot Connector

Connector type: 2x82 164-pin header
Connector location: CN15, CN19, CN22 and CN27



Pin	Definition	Pin	Definition
OA1	PE_SLOT_RST2_N	OB1	NO USE
OA2	PE_SLOT_RST3_N	OB2	NO USE
OA3	IRQ_LVC3_WAKE_N	OB3	NO USE
OA4	NO USE	OB4	NC
OA5	NO USE	OB5	NO USE
OA6	NO USE	OB6	NO USE
OA7	NO USE	OB7	NO USE
OA8	NO USE	OB8	NO USE
OA9	NO USE	OB9	NO USE
OA10	GND	OB10	GND
OA11	PE_SLOT_CLK3_DN	OB11	PE_SLOT_CLK2_DN
OA12	PE_SLOT_CLK3_DP	OB12	PE_SLOT_CLK2_DP
OA13	GND	OB13	GND
OA14	NO USE	OB14	NO USE
A1	GND	B1	P12V
A2	GND	B2	P12V
A3	GND	B3	P12V
A4	GND	B4	P12V

Pin	Definition	Pin	Definition
A5	GND	B5	P12V
A6	GND	B6	P12V
A7	SLOT_R_SCL	B7	NO USE
A8	SLOT_R_SDA	B8	NO USE
A9	NO USE	B9	NO USE
A10	GND	B10	PE_SLOT_RST0_N
A11	PE_SLOT_RST1_N	B11	P3V3_SLOT
A12	NO USE	B12	NO USE
A13	GND	B13	GND
A14	PE_SLOT_CLK1_DN	B14	PE_SLOT_CLK0_DN
A15	PE_SLOT_CLK1_DP	B15	PE_SLOT_CLK0_DP
A16	GND	B16	GND
A17	PE_SLOT_RX_DN0	B17	PE_SLOT_TX_C_DN0
A18	PE_SLOT_RX_DP0	B18	PE_SLOT_TX_C_DP0
A19	GND	B19	GND
A20	PE_SLOT_RX_DN1	B20	PE_SLOT_TX_C_DN1
A21	PE_SLOT_RX_DP1	B21	PE_SLOT_TX_C_DP1
A22	GND	B22	GND

Pin	Definition	Pin	Definition
A23	PE_SLOT_RX_DN2	B23	PE_SLOT_TX_C_DN2
A24	PE_SLOT_RX_DP2	B24	PE_SLOT_TX_C_DP2
A25	GND	B25	GND
A26	PE_SLOT_RX_DN3	B26	PE_SLOT_TX_C_DN3
A27	PE_SLOT_RX_DP3	B27	PE_SLOT_TX_C_DP3
A28	GND	B28	GND
A29	GND	B29	GND
A30	PE_SLOT_RX_DN4	B30	PE_SLOT_TX_C_DN4
A31	PE_SLOT_RX_DP4	B31	PE_SLOT_TX_C_DP4
A32	GND	B32	GND
A33	PE_SLOT_RX_DN5	B33	PE_SLOT_TX_C_DN5
A34	PE_SLOT_RX_DP5	B34	PE_SLOT_TX_C_DP5
A35	GND	B35	GND
A36	PE_SLOT_RX_DN6	B36	PE_SLOT_TX_C_DN6
A37	PE_SLOT_RX_DP6	B37	PE_SLOT_TX_C_DP6
A38	GND	B38	GND
A39	PE_SLOT_RX_DN7	B39	PE_SLOT_TX_C_DN7
A40	PE_SLOT_RX_DP7	B40	PE_SLOT_TX_C_DP7
A41	GND	B41	GND
A42	NO USE	B42	NO USE
A43	GND	B43	GND
A44	PE_SLOT_RX_DN8	B44	PE_SLOT_TX_C_DN8
A45	PE_SLOT_RX_DP8	B45	PE_SLOT_TX_C_DP8
A46	GND	B46	GND

Pin	Definition	Pin	Definition
A47	PE_SLOT_RX_DN9	B47	PE_SLOT_TX_C_DN9
A48	PE_SLOT_RX_DP9	B48	PE_SLOT_TX_C_DP9
A49	GND	B49	GND
A50	PE_SLOT_RX_DN10	B50	PE_SLOT_TX_C_DN10
A51	PE_SLOT_RX_DP10	B51	PE_SLOT_TX_C_DP10
A52	GND	B52	GND
A53	PE_SLOT_RX_DN11	B53	PE_SLOT_TX_C_DN11
A54	PE_SLOT_RX_DP11	B54	PE_SLOT_TX_C_DP11
A55	GND	B55	GND
A56	PE_SLOT_RX_DN12	B56	PE_SLOT_TX_C_DN12
A57	PE_SLOT_RX_DP12	B57	PE_SLOT_TX_C_DP12
A58	GND	B58	GND
A59	PE_SLOT_RX_DN13	B59	PE_SLOT_TX_C_DN13
A60	PE_SLOT_RX_DP13	B60	PE_SLOT_TX_C_DP13
A61	GND	B61	GND
A62	PE_SLOT_RX_DN14	B62	PE_SLOT_TX_C_DN14
A63	PE_SLOT_RX_DP14	B63	PE_SLOT_TX_C_DP14
A64	GND	B64	GND
A65	PE_SLOT_RX_DN15	B65	PE_SLOT_TX_C_DN15
A66	PE_SLOT_RX_DP15	B66	PE_SLOT_TX_C_DP15
A67	GND	B67	GND
A68		B68	
A69		B69	
A70	NO USE	B70	NO USE

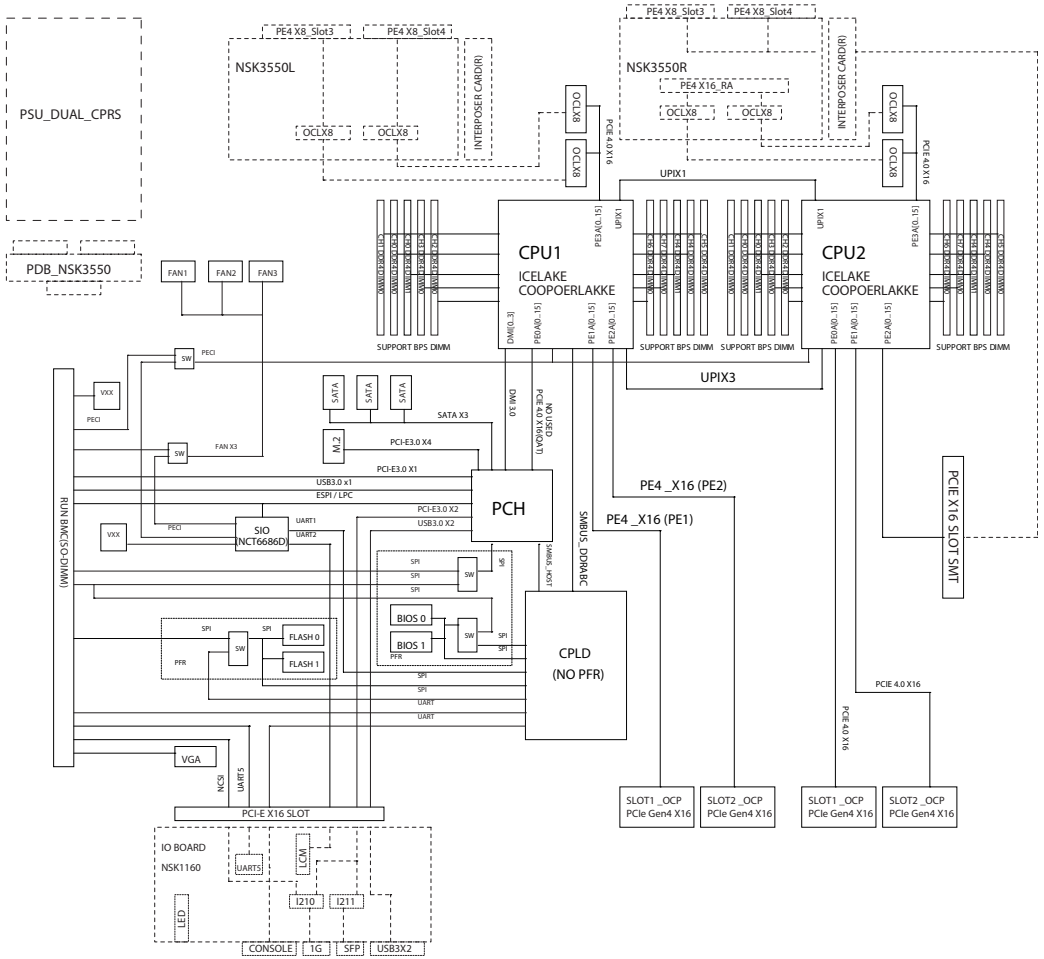
M.2 Connector (M Key)

Connector type: NGFF M Key 2280
Connector location: CN4

Pin	Definition	Pin	Definition
1	NGFF_CONFIG_3	2	P3V3
3	GND	4	P3V3
5	PCIE_RX_M2_R_3_DN	6	NC
7	PCIE_RX_M2_R_3_DP	8	NC
9	GND	10	NGFF_DSSN
11	PCIE_TX_M2_R_3_DN	12	P3V3
13	PCIE_TX_M2_R_3_DP	14	P3V3
15	GND	16	P3V3
17	PCIE_RX_M2_R_2_DN	18	P3V3
19	PCIE_RX_M2_R_2_DP	20	NC
21	NGFF_CONFIG_0	22	NC
23	PCIE_TX_M2_R_2_DN	24	NC
25	PCIE_TX_M2_R_2_DP	26	NC
27	GND	28	NC
29	PCIE_RX_M2_R_1_DN	30	NC
31	PCIE_RX_M2_R_1_DP	32	NC
33	GND	34	NC

Pin	Definition	Pin	Definition
35	PCIE_TX_M2_R_1_DN	36	NC
37	PCIE_TX_M2_R_1_DP	38	NGFF_DEVSLP
39	GND	40	N30398252
41	PCIE_RX_M2_R_0_DN	42	N30398249
43	PCIE_RX_M2_R_0_DP	44	NC
45	GND	46	NC
47	PCIE_TX_M2_R_0_DN	48	NC
49	PCIE_TX_M2_R_0_DP	50	PE_RST_M2_N
51	GND	52	FM_CLKREQ_M2_1_N
53	CLK_100M_M2_DN	54	IRQ_LVC3_WAKE_N
55	CLK_100M_M2_DP	56	NC
57	GND	58	NC
67	NC	68	PCH_SUSCLK_33K_R_SSD
69	FM_M2_1_PEDET	70	P3V3
71	GND	72	P3V3
73	GND	74	P3V3
75	NGFF_CONFIG_2		

Block Diagram



Chapter 3: System Setup

Removing the Chassis Cover

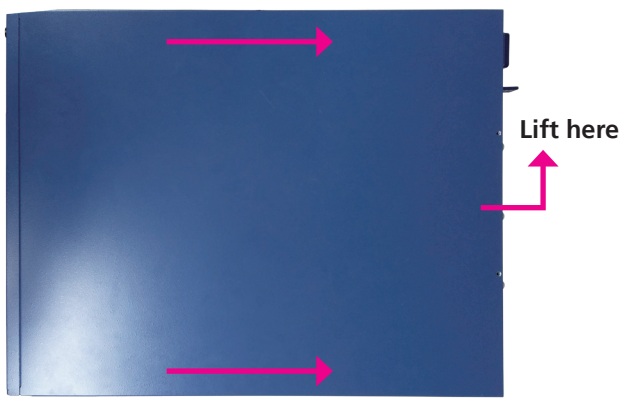
Prior to removing the chassis cover, make sure the unit's power is off and disconnected from the power sources to prevent electric shock or system damage.

1. The screws on the bottom and sides are used to secure the cover to the chassis. Remove these screws and put them in a safe place for later use.

Screws on the sides

Screws on the top

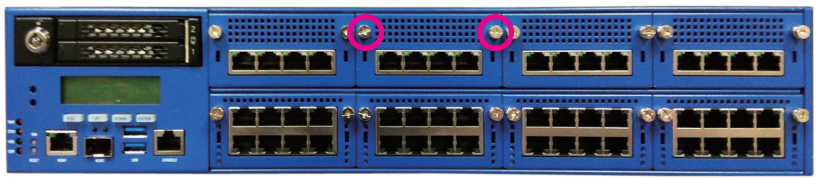
2. With the screws removed, gently slide the cover outwards and then lift up the cover to remove it.



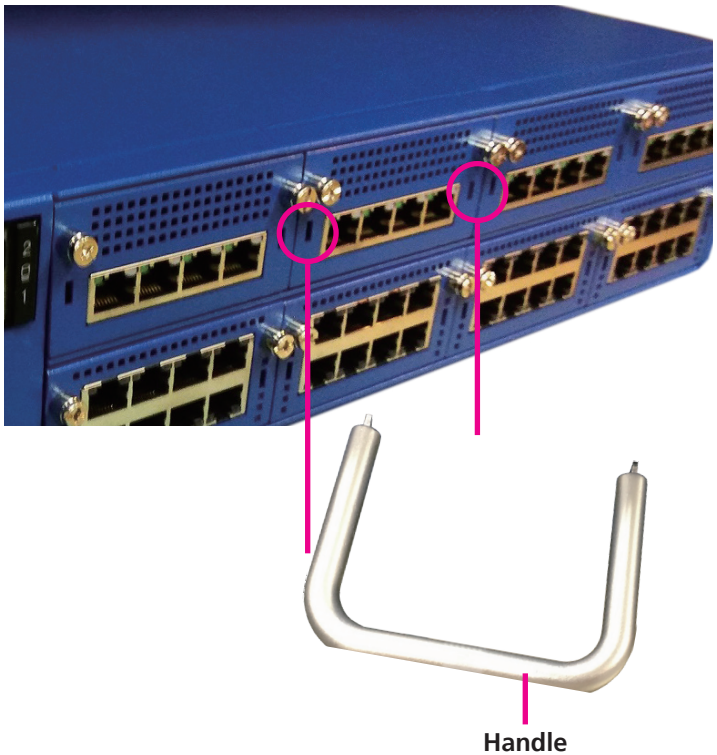
Installing a LAN Module

Please correctly follow the below instructions and noted items to avoid making unnecessary damages. Make sure the power supply is switched off and disconnected from the power sources before replacing or adding LAN modules to prevent electric shock or system damage.

1. Loosen the two screws on the LAN module.

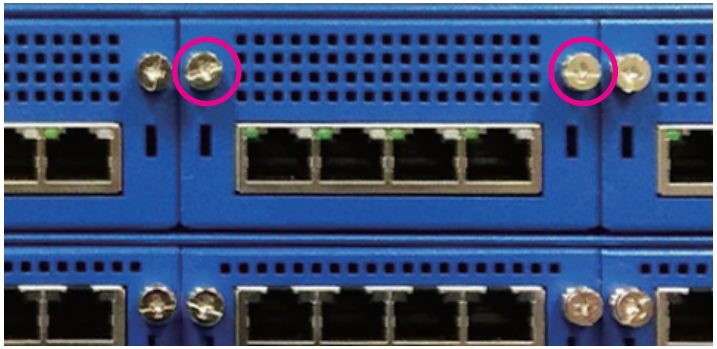


2. Use the handle provided, and insert the handle into the two holes on the LAN module.



3. Once the handle is firmly secured in position, pull the handle outwards to remove the LAN module.

4. Insert the new LAN module into the slot and secure the module with the two screws.



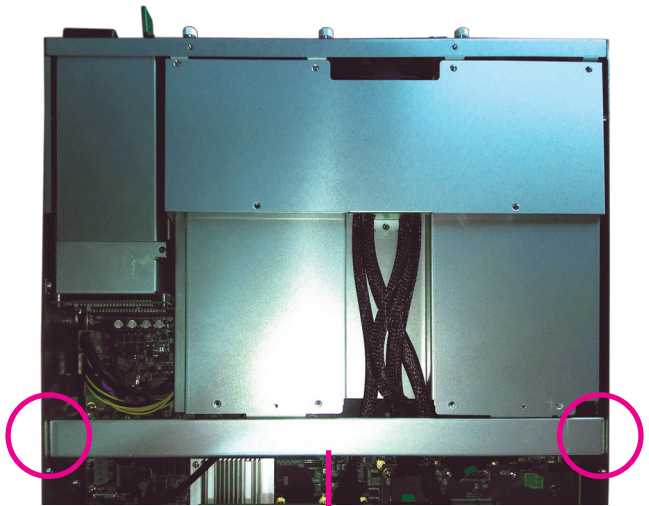
Important:
Before using Optical fiber for transferring data, make sure you have connected an approved Optical Transceiver Module. User needs to install appropriate and UL approved Laser Class I Transceivers, rated 3.3Vdc, max. 1W.

Installing a CPU

The CPU sockets are covered by 3 covers consisting of the front cover, rear cover and middle cover. To access the CPU sockets, the 3 covers need to be removed first. The following instructions explain how to remove the 3 covers.

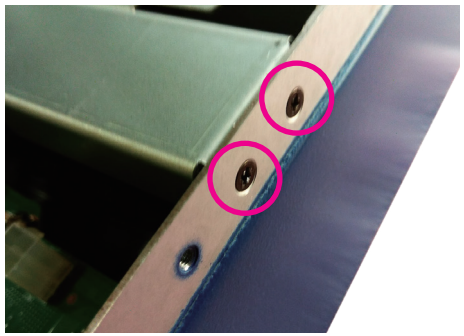
Removing the Front Cover

1. With the chassis cover removed, locate the front cover and remove the screws on the left and right side of the cover.

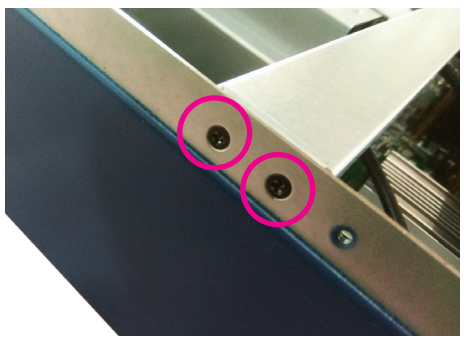


Front Cover

Right Side

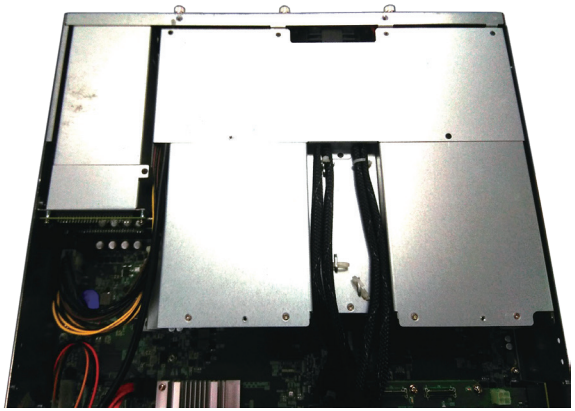


Left Side



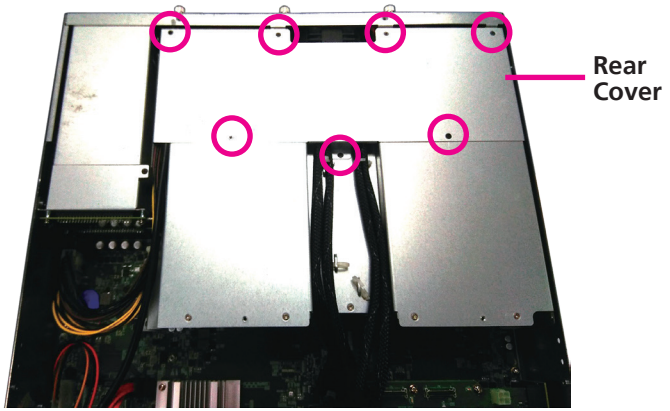
Before installing or removing internal components on the mainboard, please ensure that the AC power cord is unplugged for at least over 10 seconds.

2. Remove the front cover.

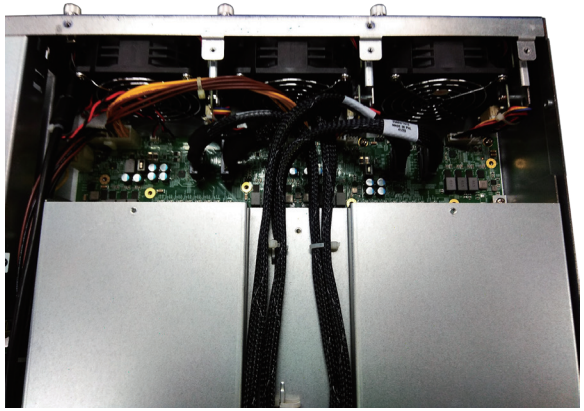


Removing the Rear Cover

1. Locate the rear cover and remove the screws securing it as shown below.

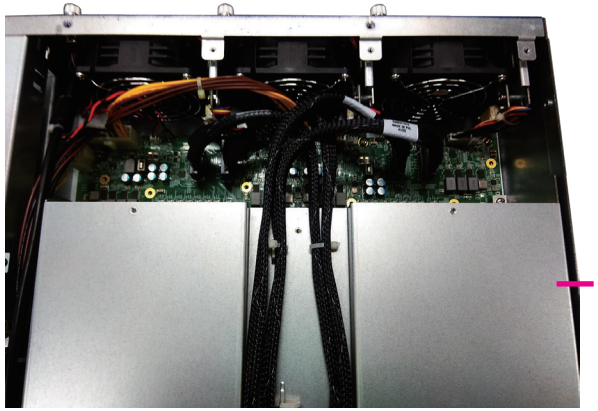


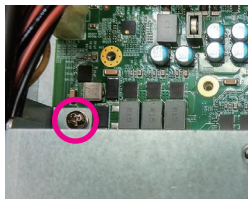
2. Remove the rear cover.

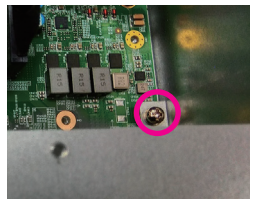


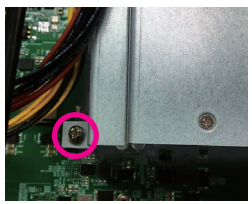
Removing the Middle Cover

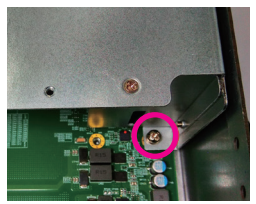
1. Locate and remove the screws on the four corners of the middle cover.



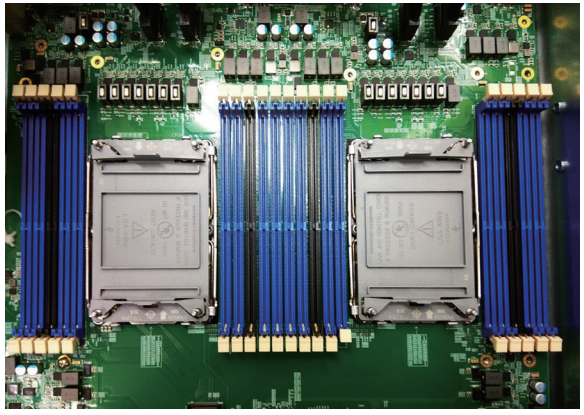






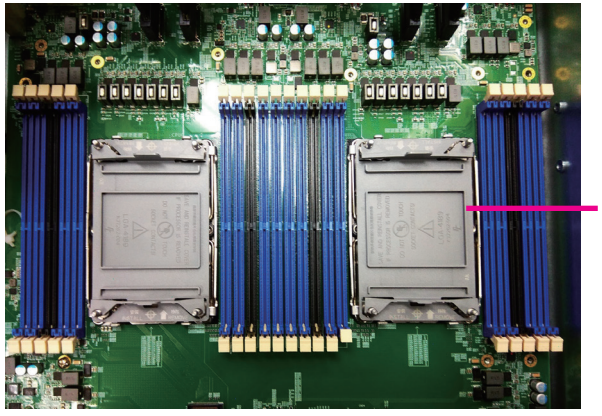


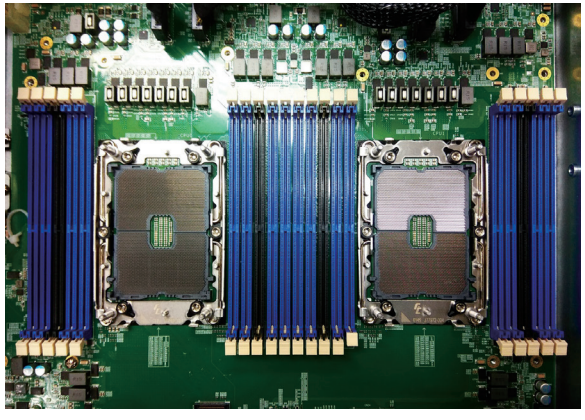
2. Remove the middle cover to access the CPU sockets.



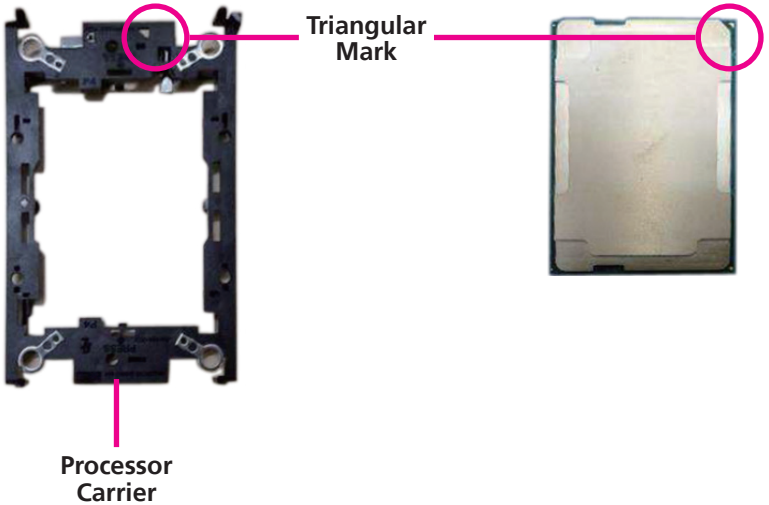
Installing the CPU

1. Remove the protective cap on the CPU socket.

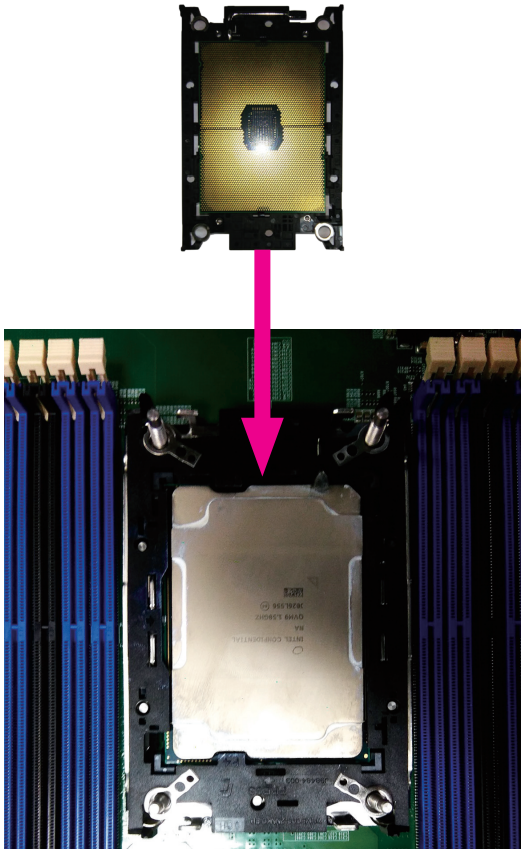




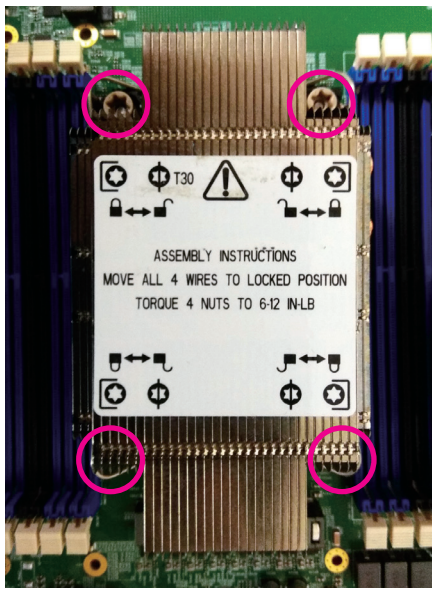
2. Place the CPU into the processor carrier with the triangular mark on the CPU aligned to the triangular mark (pin 1 indicator) on the processor carrier.



3. With the CPU placed into the processor carrier, install the CPU onto the CPU socket.

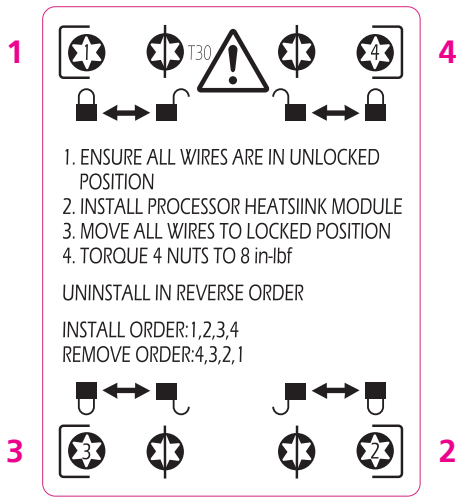


4. Place the heat sink on top of the CPU with the screws aligned to the four corners of the processor carrier, then secure the screws using a T30 screwdriver. Make sure to tighten the screws with a torque of 6-12 IN-LB.



Please ensure that the T30 screws are tightened with a torque of 6-12 IN-LB. Otherwise, the motherboard may be damaged.

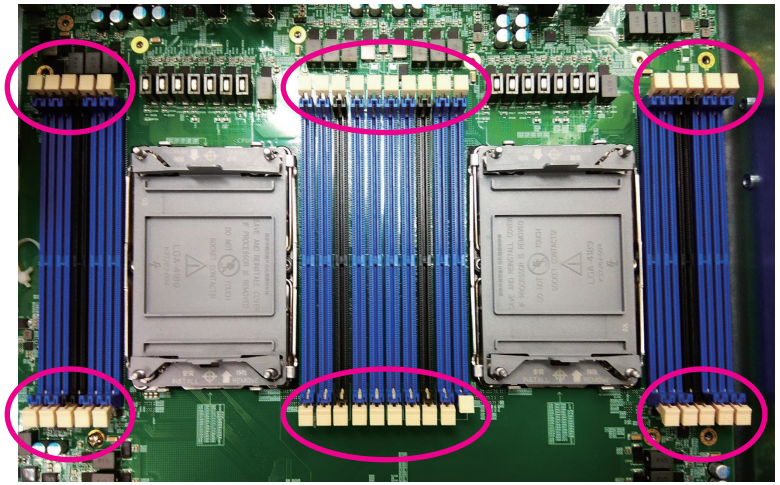
5. Secure the four screws in the following order: 1, 2, 3 and 4.



To uninstall the heat sink, remove the screws in reverse order: 4, 3, 2 and 1.

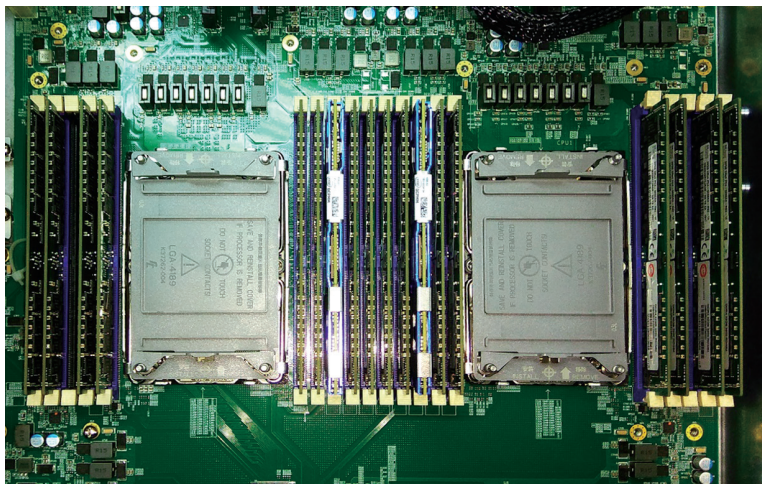
Installing Memory Modules

1. Locate the DIMM sockets on the motherboard and release the locks.



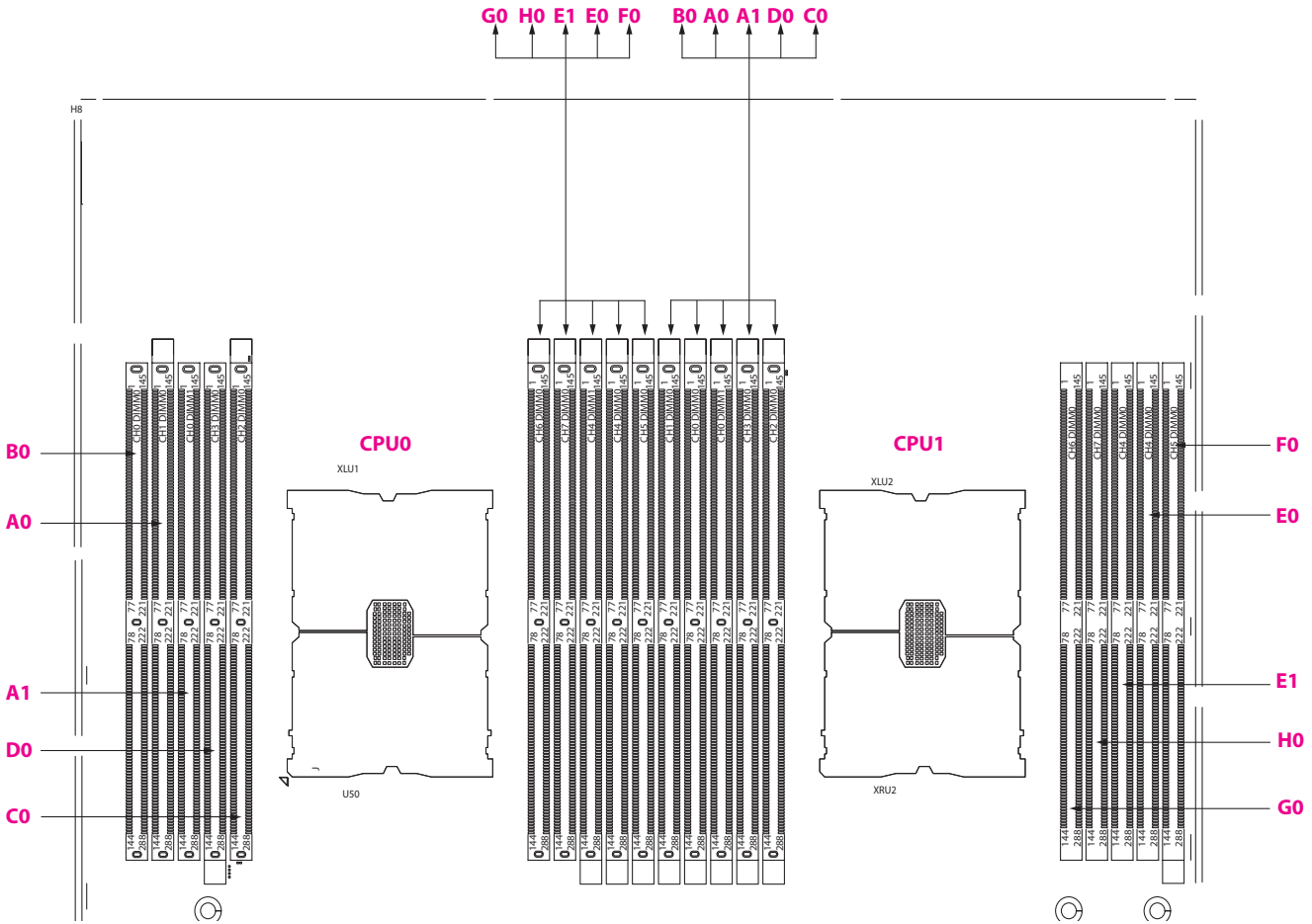
Before installing or removing internal components on the mainboard, please ensure that the AC power cord is unplugged for at least over 10 seconds.

2. Insert the module into the socket at an 90 degree angle. Apply firm even pressure to each end of the module until it slips into the socket. While pushing the module into position, the locks will close automatically.



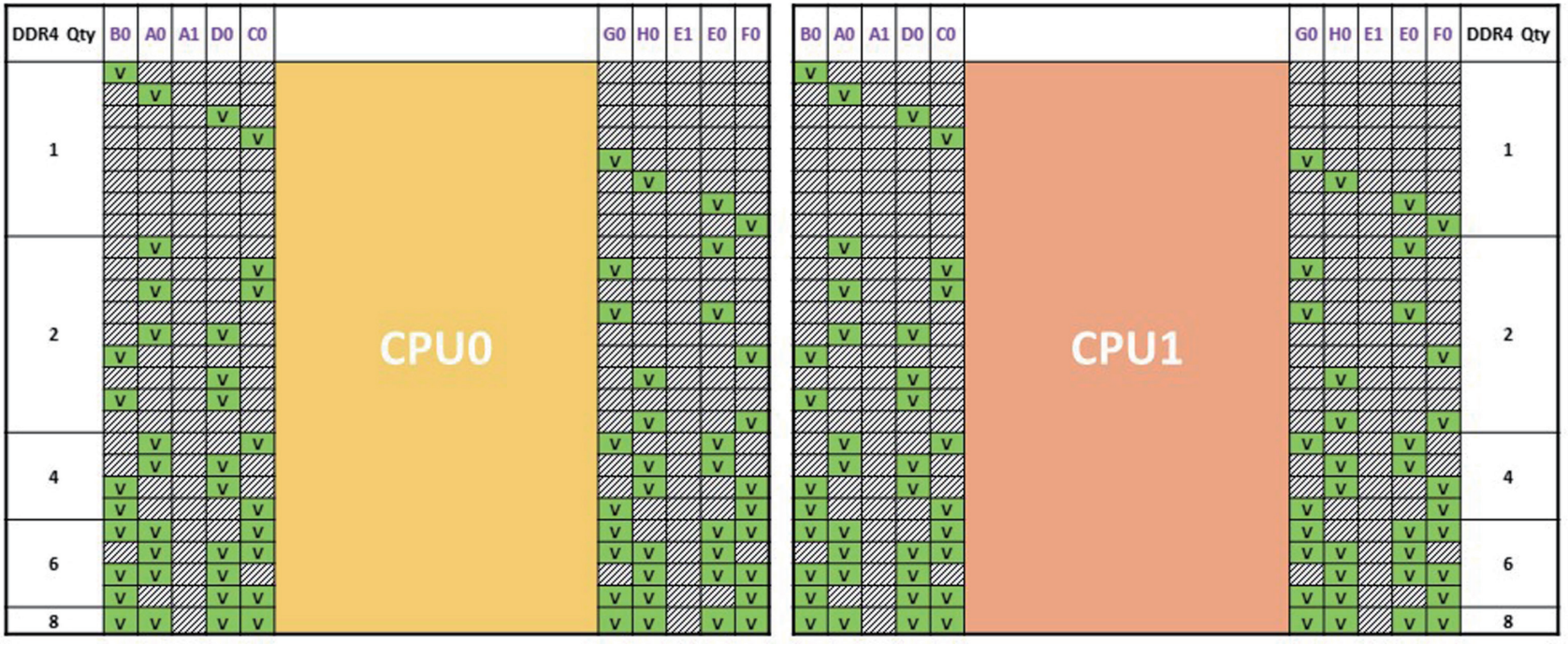
Note: For information on the memory population rule, please refer to pages 48 and 49.

CPU and Memory Layout



DDR4 Memory Population Table

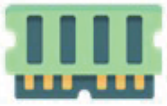
DDR4 memory population table for the 3rd Gen Intel® Xeon® Scalable Processor is shown below.
If you use only one please refer to the table of corresponding color (yellow for CPU0 and orange for CPU1)



DDR4 and Intel® Optane™ Persistent Memory Population Table

DDR4+BSP memory population table for the 3rd Gen Intel® Xeon® Scalable Processor is shown below.
If you use only one please refer to the table of corresponding color (yellow for CPU0 and orange for CPU1)

Note:

DDR4 Memory 

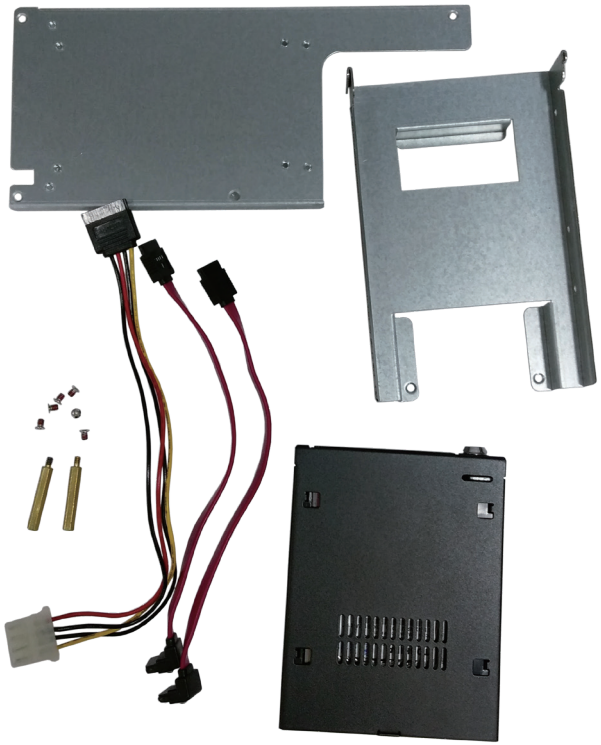
Intel® Optane™ Persistent Memory, Barlow Pass (BPS) 

DDR4+BPS Qty	B0	A0	A1	D0	C0	CPU0	G0	H0	E1	E0	F0
4+4	V	V		V	V		V	V		V	V
	V	V		V	V		V	V		V	V
6+1	V	V		V	V		V			V	V
	V	V		V	V		V	V		V	
	V	V			V		V	V		V	M
		V		V	V		V	V		V	V
	V	V		V	V			V		V	V
	V	V		V	V		V	V			V
	V	V		V			V	V		V	V
	V			V	V		V	V		V	V
8+1	V	V	V	V	V		V	V		V	V
	V	V		V	V		V	V	V	V	M

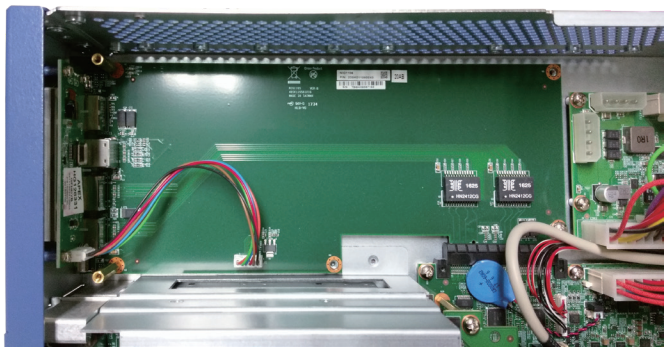
B0	A0	A1	D0	C0	CPU1	G0	H0	E1	E0	F0	DDR4+BPS Qty
V	V		V	V		V	V		V	V	4+4
V	V		V	V		V	V		V	V	
V	V		V	V		V			V	V	6+1
V	V		V	V		V	V		V		
V	V			V		V	V		V	M	
	V		V	V		V	V		V	V	
V	V		V	V			V		V	V	
V	V		V	V		V	V			V	
V	V		V			V	V		V	V	
V			V	V		V	V		V	V	
V	V	V	V	V		V	V		V	V	8+1
V	V		V	V		V	V	V	V	M	

Assembling the 2.5” Removable Drive Bay

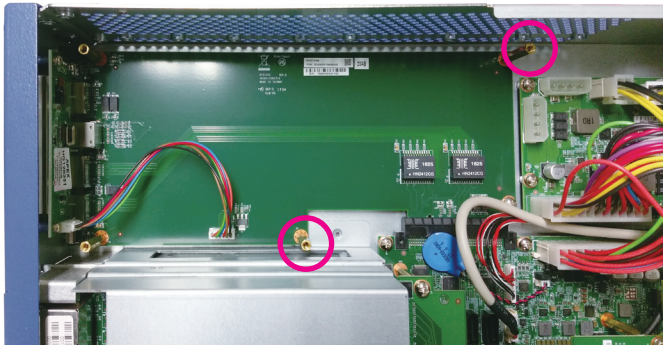
The 2.5” removable drive bay kit contains the parts pictured below:



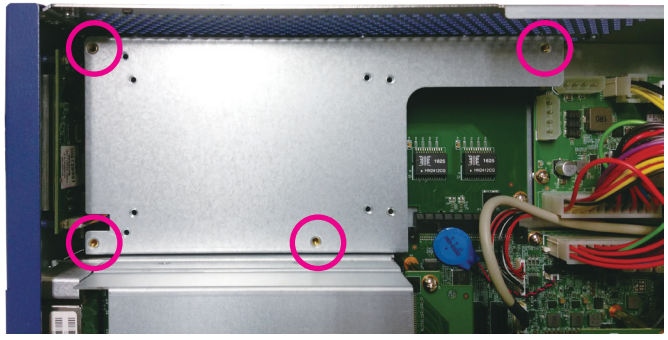
1. Locate the installation location for the drive bay kit.



2. Install the two copper standoffs to the location circled below.

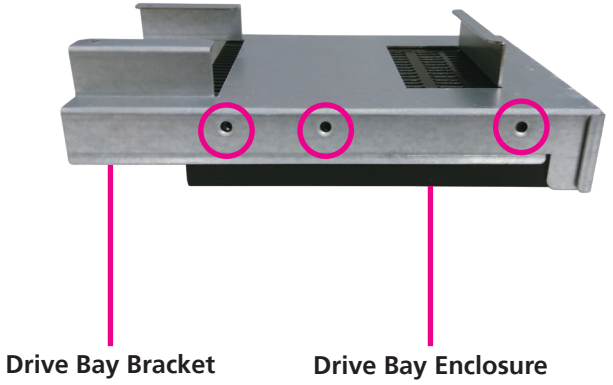


3. Align the mounting holes on the base plate to the copper standoffs.

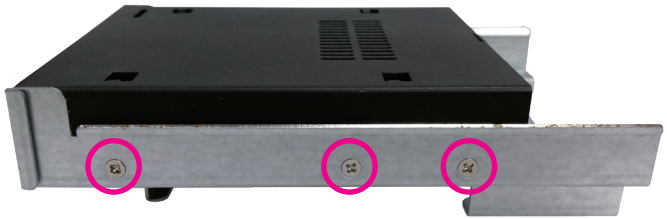


4. Secure the base plate to the standoffs with screws.

5. Align the mounting holes on the drive bay enclosure to the mounting holes on the drive bay bracket.

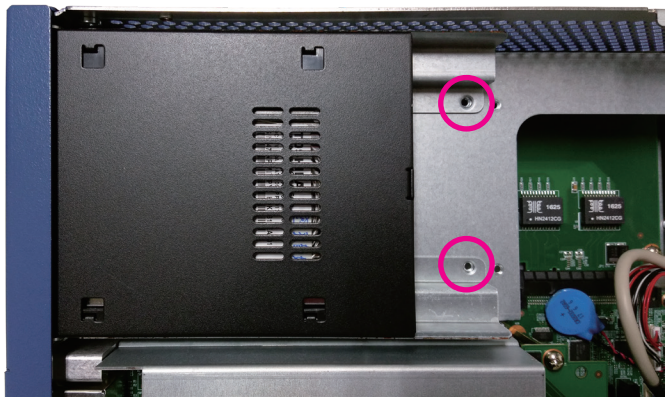


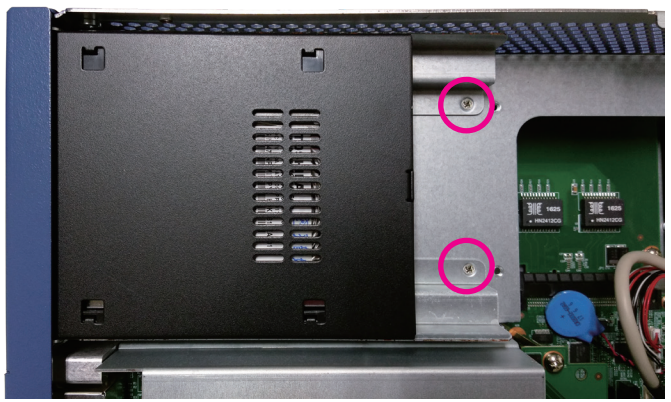
6. Secure the drive bay enclosure to the bracket with screws.



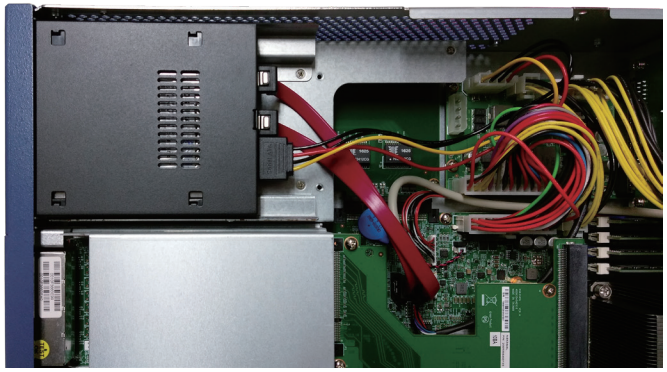
7. Repeat step 6 for securing the screws on the other side of the bracket.

8. Fix the drive bay bracket to the base plate with screws.



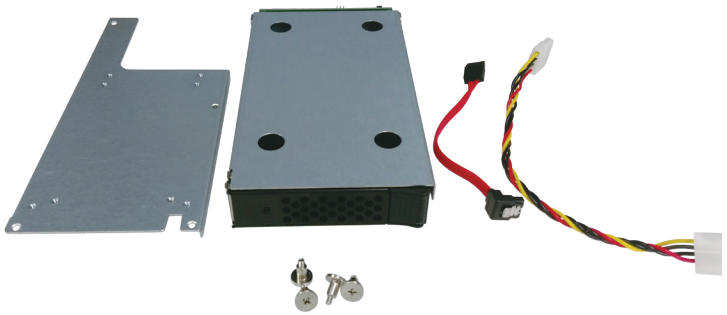


9. Connect the SATA data and power cables to the respective connectors on the board and the other ends of the cables to the connectors on the drive bay enclosure.

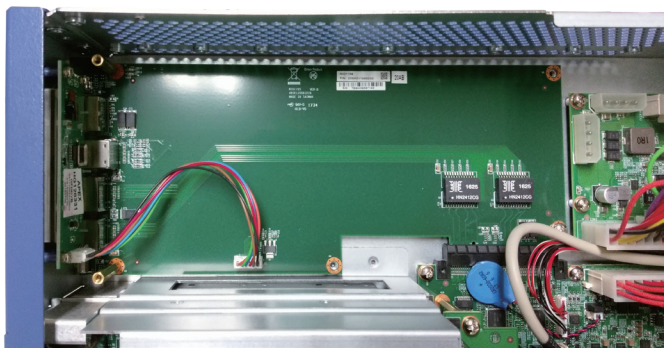


Assembling the 3.5” Removable Drive Bay

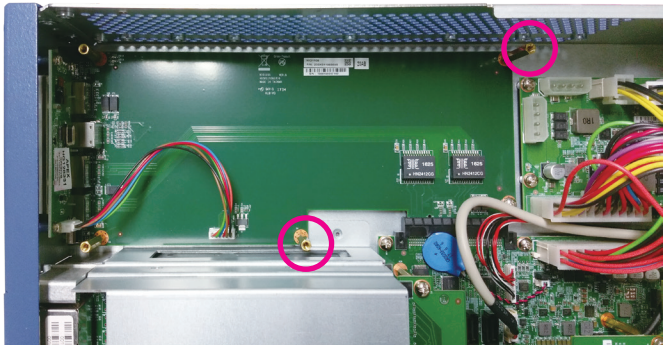
The 3.5” removable drive bay kit contains the parts pictured below:



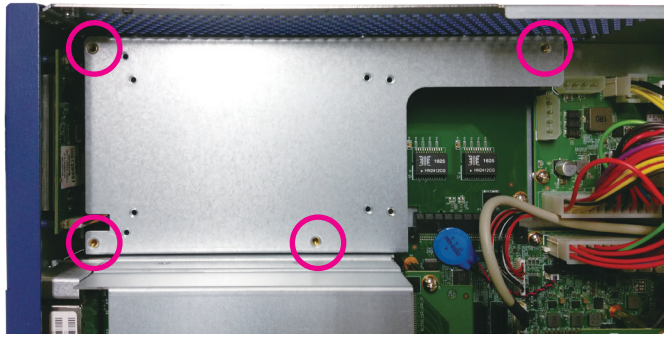
1. Locate the installation location for the drive bay kit.



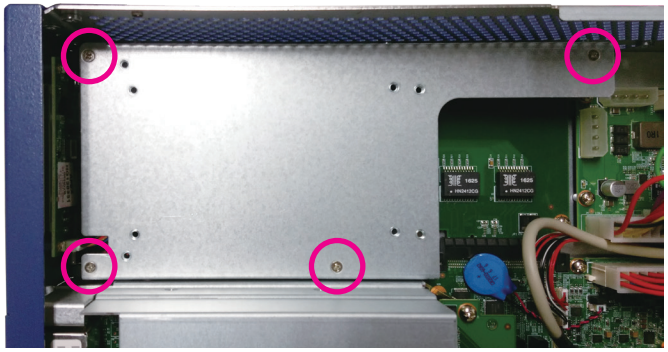
2. Install the two copper standoffs to the location circled below.



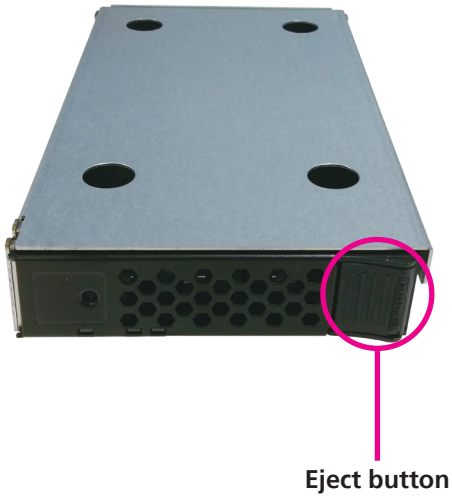
3. Align the mounting holes on the base plate to the copper standoffs.



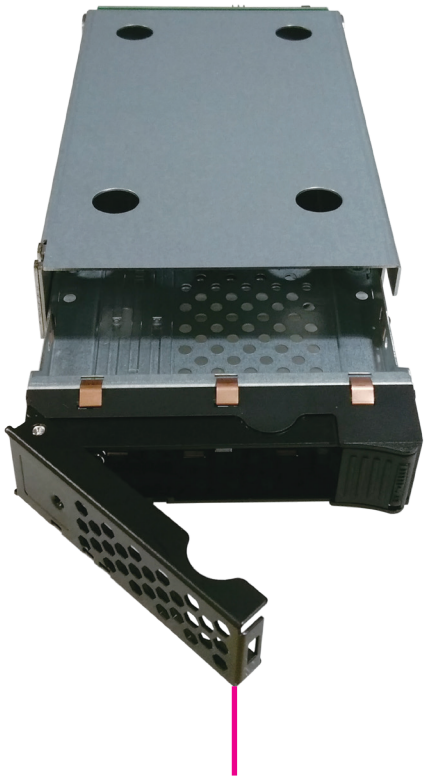
4. Secure the base plate to the standoffs with screws.



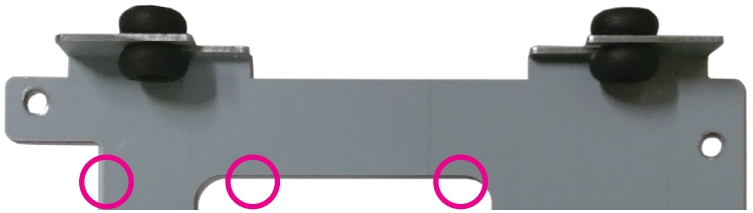
5. Push the eject button on the HDD drive tray to release the latch.



6. Grab on the latch and pull the drive tray out gently.



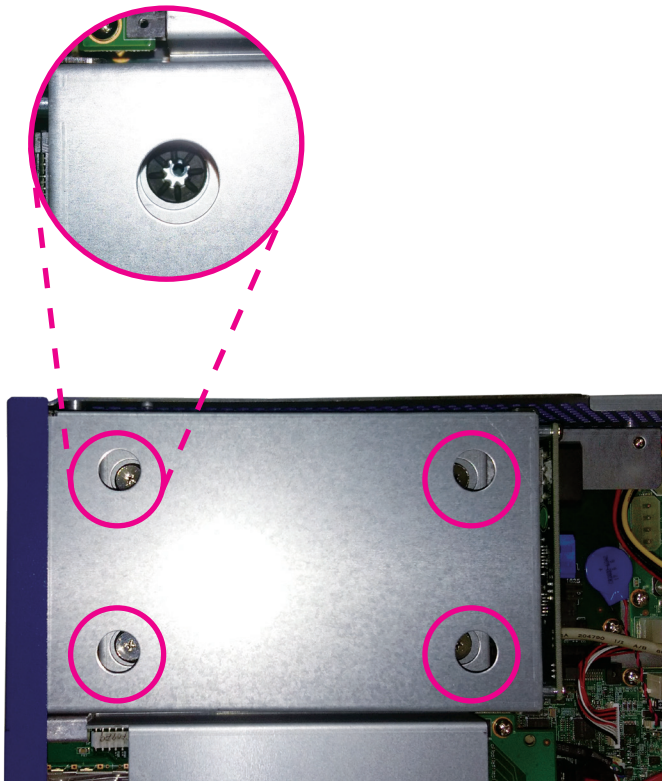
7. Place the SATA drive onto the tray and align the mounting holes on the drive with the mounting holes on the tray, then secure the drive in place with screws.



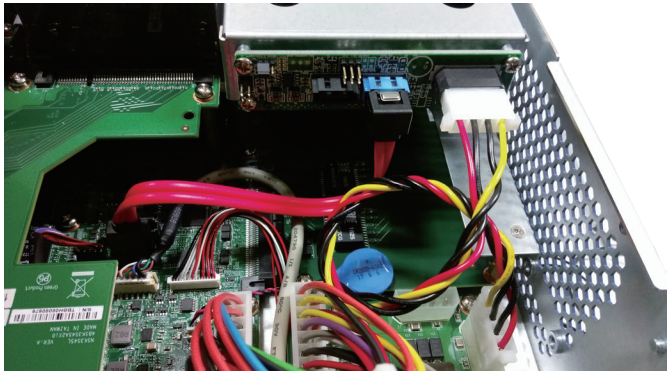
8. Repeat step 7 for securing the screws on the other side of the HDD tray.

9. Slide the tray back into the drive bay enclosure, and push firmly until you hear a distinctive click sound.

10. Fix the drive bay enclosure to the base plate with screws.



11. Connect the SATA data and power cables to the respective connectors on the board and the other ends of the cables to the connectors on the drive bay enclosure.



Chapter 4: BIOS Setup

This chapter describes how to use the BIOS setup program for NSA 7150/7150A. The BIOS screens provided in this chapter are for reference only and may change if the BIOS is updated in the future.

To check for the latest updates and revisions, visit the NEXCOM website at www.nexcom.com.tw.

About BIOS Setup

The BIOS (Basic Input and Output System) Setup program is a menu driven utility that enables you to make changes to the system configuration and tailor your system to suit your individual work needs. It is a ROM-based configuration utility that displays the system's configuration status and provides you with a tool to set system parameters.

These parameters are stored in non-volatile battery-backed-up CMOS RAM that saves this information even when the power is turned off. When the system is turned back on, the system is configured with the values found in CMOS.

With easy-to-use pull down menus, you can configure such items as:

- Hard drives, diskette drives, and peripherals
- Video display type and display options
- Password protection from unauthorized use
- Power management features

The settings made in the setup program affect how the computer performs. It is important, therefore, first to try to understand all the setup options, and second, to make settings appropriate for the way you use the computer.

When to Configure the BIOS

- This program should be executed under the following conditions:
- When changing the system configuration
- When a configuration error is detected by the system and you are prompted to make changes to the setup program
- When resetting the system clock
- When redefining the communication ports to prevent any conflicts
- When making changes to the Power Management configuration
- When changing the password or making other changes to the security setup

Normally, CMOS setup is needed when the system hardware is not consistent with the information contained in the CMOS RAM, whenever the CMOS RAM has lost power, or the system features need to be changed.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering Setup

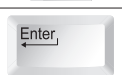
When the system is powered on, the BIOS will enter the Power-On Self Test (POST) routines. These routines perform various diagnostic checks; if an error is encountered, the error will be reported in one of two different ways:

- If the error occurs before the display device is initialized, a series of beeps will be transmitted.
- If the error occurs after the display device is initialized, the screen will display the error message.

Powering on the computer and immediately pressing 

allows you to enter Setup.

Legends

Key	Function
	Moves the highlight left or right to select a menu.
	Moves the highlight up or down between sub-menu or fields.
	Exits the BIOS Setup Utility.
	Scrolls forward through the values or options of the highlighted field.
	Scrolls backward through the values or options of the highlighted field.
	Selects a field.
	Displays General Help.
	Load previous values.
	Load optimized default values.
	Saves and exits the Setup program.
	Press <Enter> to enter the highlighted sub-menu

Scroll Bar

When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu

When "▶" appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press 

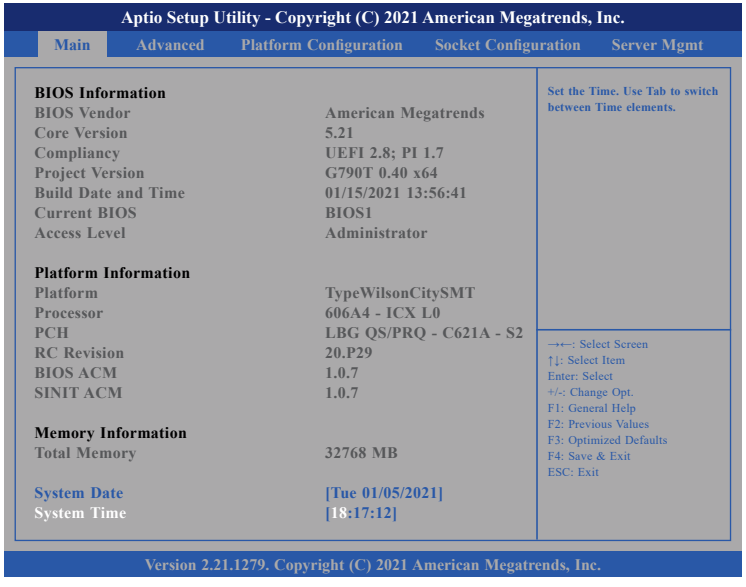
.

BIOS Setup Utility

Once you enter the AMI BIOS Setup Utility, the Main Menu will appear on the screen. The main menu allows you to select from several setup functions and one exit. Use arrow keys to select among the items and press Enter to accept or enter the submenu.

Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <day>, <month>, <date>, <year>. Day displays a day, from Monday to Sunday. Month displays the month, from January to December. Date displays the date, from 1 to 31. Year displays the year, from 1998 to 9999.

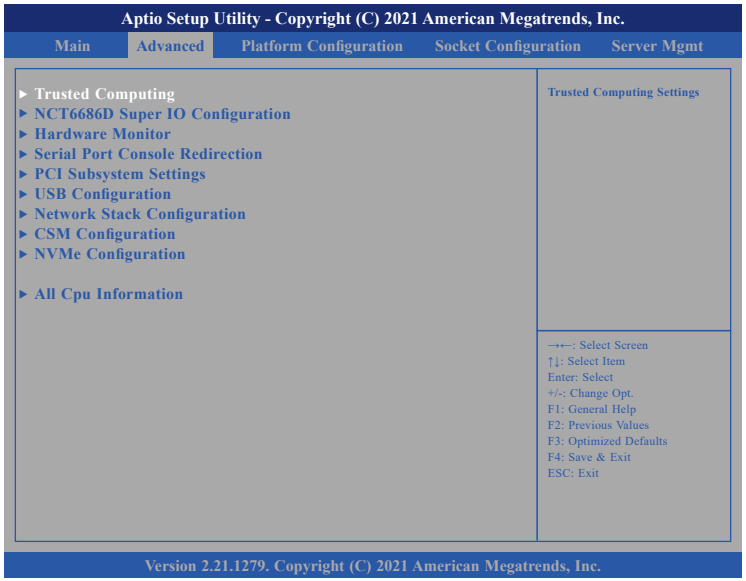
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

Advanced

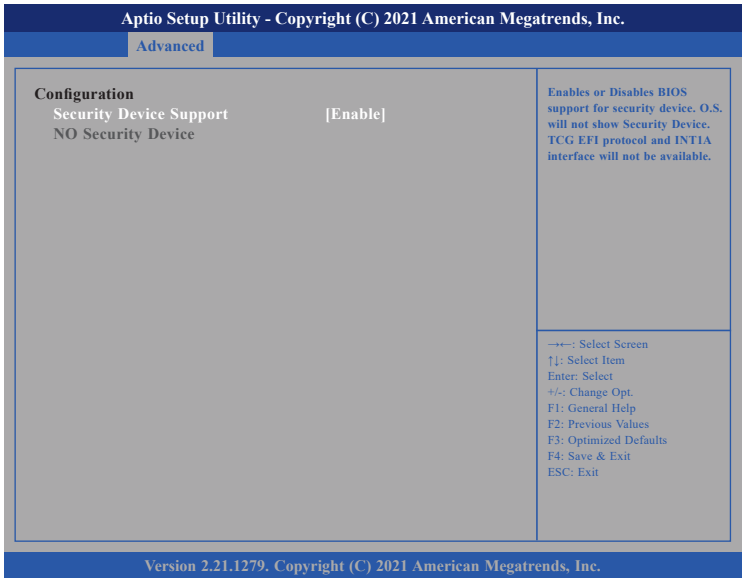
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Setting incorrect field values may cause the system to malfunction.



Trusted Computing

This section is used to configure Trusted Platform Module (TPM) settings.



Security Device Support

Enables or disables BIOS support for security device. O.S will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

NCT6686D Super IO Configuration

This section is used to configure the serial port.

Super IO Chip

Displays the Super I/O chip used on the board.

Serial Port 1 Configuration

Configuration settings for serial port 1.

Serial Port 2 Configuration

Configuration settings for serial port 2.

Serial Port 1 Configuration

This section is used to configure serial port 1.

Serial Port

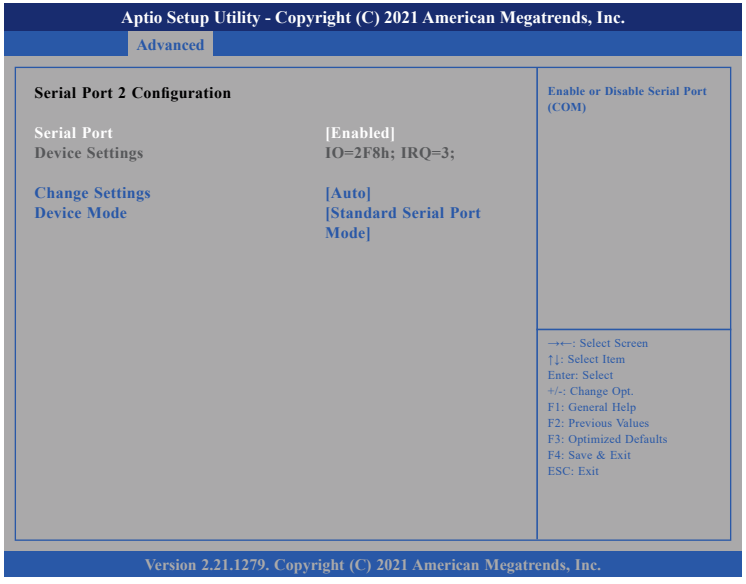
Enables or disables the serial port.

Change Settings

Selects an optimal setting for the Super IO device.

Serial Port 2 Configuration

This section is used to configure serial port 2.



Serial Port

Enables or disables the serial port.

Change Settings

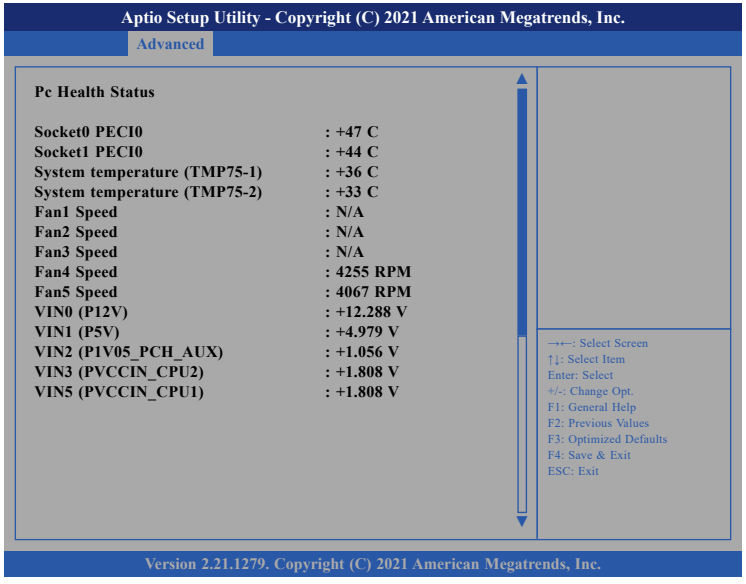
Selects an optimal setting for the Super IO device.

Device Mode

Configures the operating mode of the serial port.

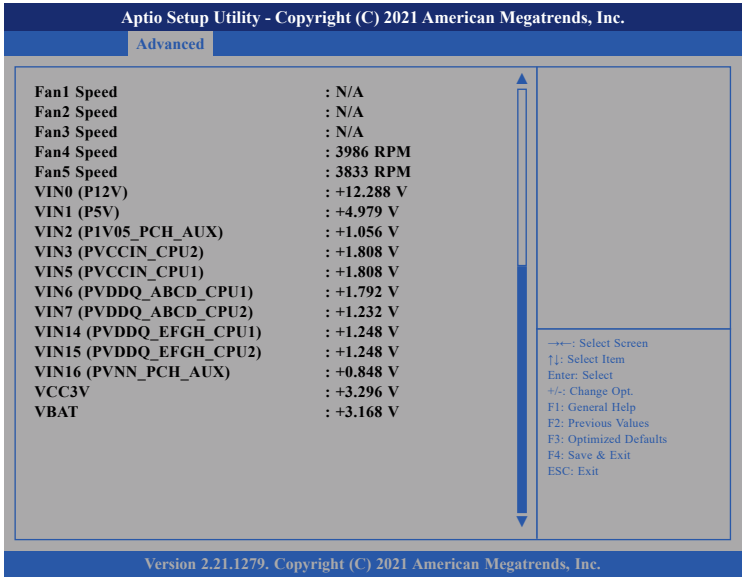
Hardware Monitor

This section is used to monitor hardware status such as temperature, fan speed and voltages.



Socket0 PECI0 to VIN5 (PVCCIN_CPU1)

Detects and displays the temperatures, fan speeds and output voltages.

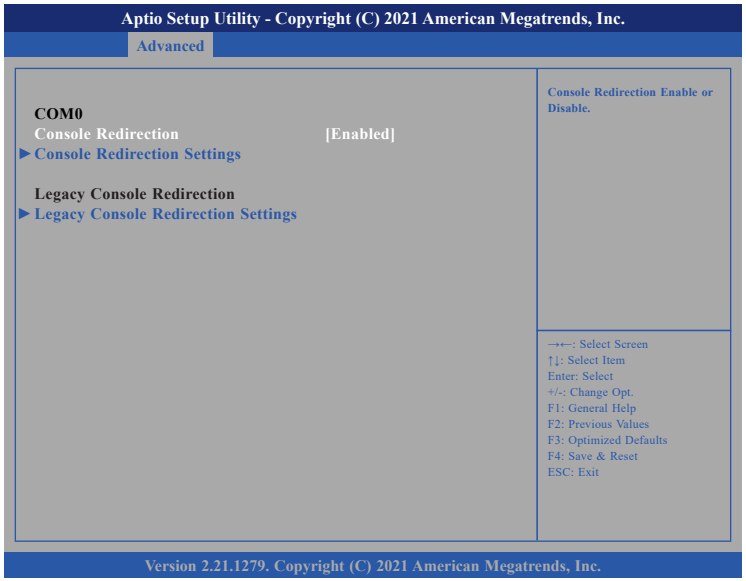


Fan1 Speed to VBAT

Detects and displays the fan speeds and output voltages.

Serial Port Console Redirection

This section is used to configure the serial port that will be used for console redirection.

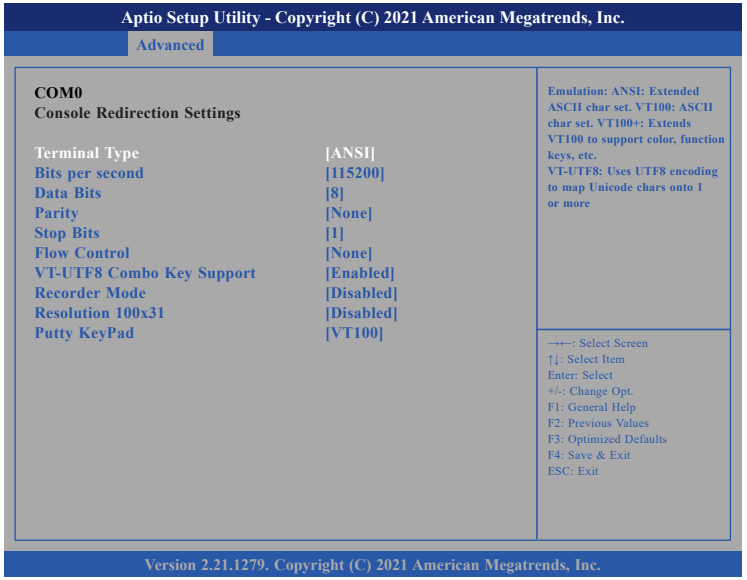


Console Redirection

Enables or disables console redirection for COM0.

Console Redirection Settings (COM0)

Specifies how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.



Terminal Type

ANSI Extended ASCII character set.
VT100 ASCII character set.
VT100+ Extends VT100 to support color, function keys, etc.
VT-UTF8 Uses UTF8 encoding to map Unicode characters onto 1 or more bytes.

Bits Per Second

Selects the serial port transmission speed. The speed must match the other side. Long or noisy lines may require a lower speed.

Data Bits
The options are 7 and 8.

Parity
A parity bit can be sent with the data bits to detect some transmission errors.

Even Parity bit is 0 if the number of 1's in the data bits is even.
Odd Parity bit is 0 if number of 1's in the data bits is odd.

Stop Bits
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Flow Control
Flow control can prevent data loss from buffer overflow. When sending data and the receiving buffers are full, a "stop" signal can be sent to stop the data flow.

VT-UTF8 Combo Key Support
Enables or disables VT-UTF8 combo key support.

Recorder Mode
When this field is enabled, only text will be sent. This is to capture the terminal data.

Resolution 100x31
Enables or disables extended terminal resolution.

Putty KeyPad
Selects the Putty keyboard emulation type.

PCI Subsystem Settings

This section is used to configure the PCI.

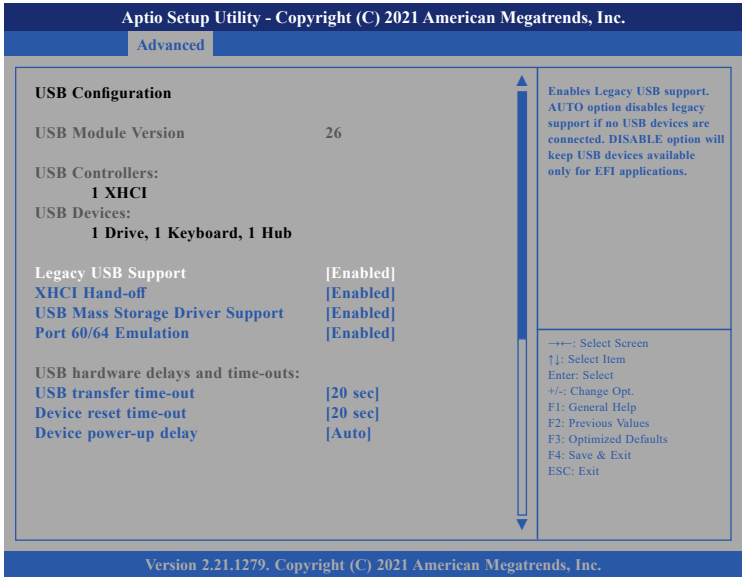
Above 4G Decoding
Enables or disables decoding of 64-bit devices in 4G address space. (Only if the system supports 64-bit PCI decoding.)

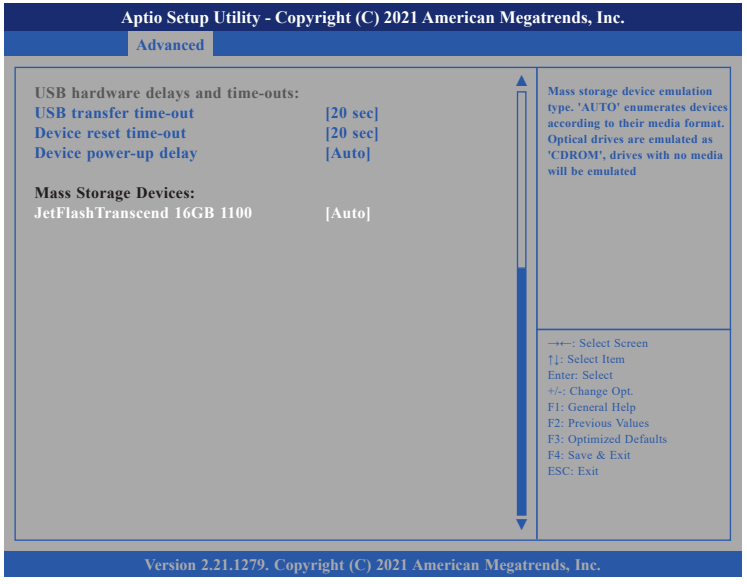
SR-IOV Support
Enables or disables SR-IOV support.

BME DMA Mitigation
Enables or disables the function to re-enable bus master attribute during PCI enumeration for PCI bridges after SMM is locked.

USB Configuration

This section is used to configure the USB.





Legacy USB Support

Enable Enables Legacy USB.
Auto Disables support for Legacy when no USB devices are connected.
Disable Keeps USB devices available only for EFI applications.

XHCI Hand-off

This is a workaround for OSs that does not support XHCI hand-off. The XHCI ownership change should be claimed by the XHCI driver.

USB Mass Storage Driver Support

Enables or disables USB mass storage device driver support.

Port 60/64 Emulation

Enables I/O port 60h/64h emulation support. This should be enabled for complete USB keyboard legacy support for non-USB aware OS.

USB transfer time-out

The time-out value for control, bulk, and Interrupt transfers.

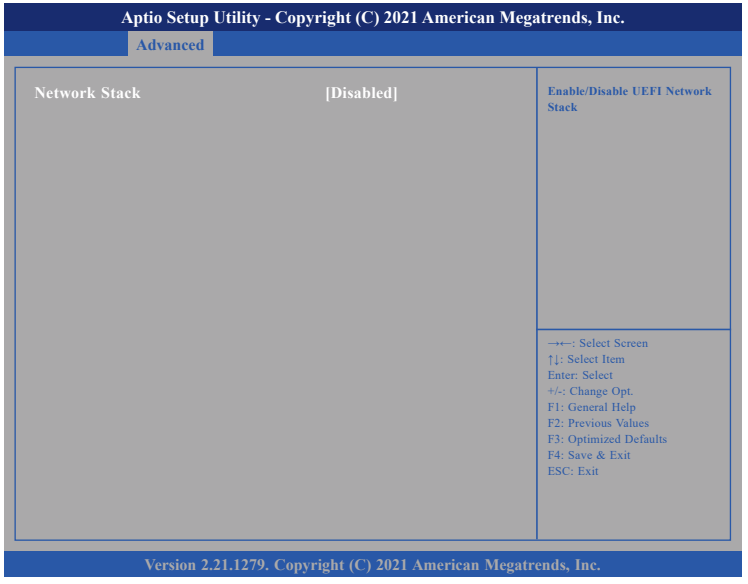
Device reset time-out
Selects the USB mass storage device's start unit command timeout.

Device power-up delay
Maximum time the value will take before it properly reports itself to the Host Controller. "Auto" uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

Mass Storage Devices:
Selects the mass storage device emulation type.

Network Stack Configuration

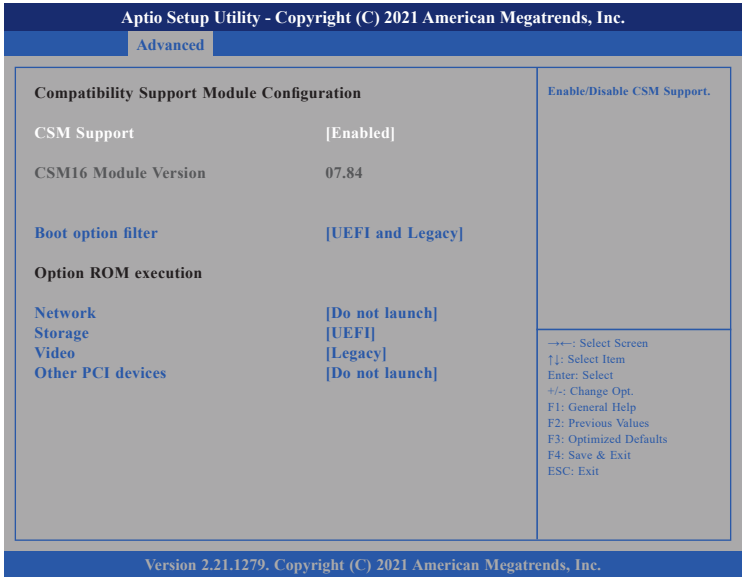
This section is used to configure the network stack.



Network Stack
Enables or disables UEFI network stack.

CSM Configuration

This section is used to configure the compatibility support module features.



Boot option filter
Configures which devices the system will boot from.

Network
Controls the execution of UEFI and Legacy PXE OpROM.

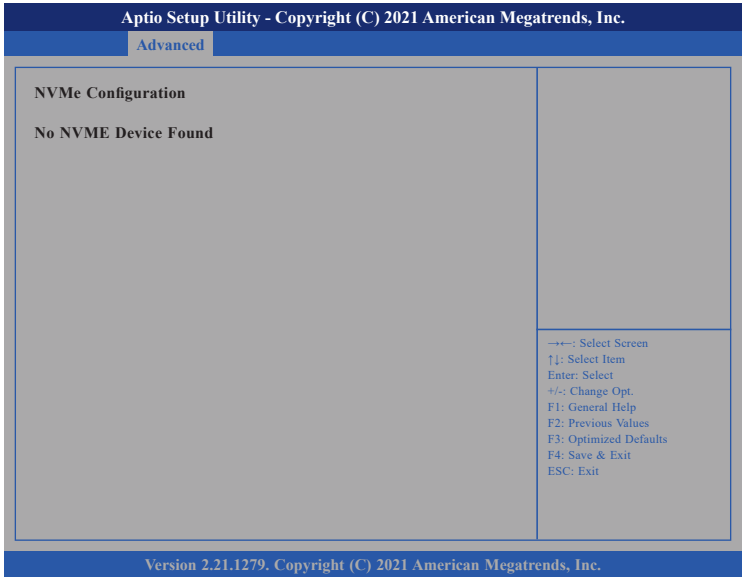
Storage
Controls the execution of UEFI and Legacy Storage OpROM.

Video
Controls the execution of UEFI and Legacy Video OpROM.

Other PCI Devices
Configures the OpROM execution policy for devices other than Network, Storage or Video.

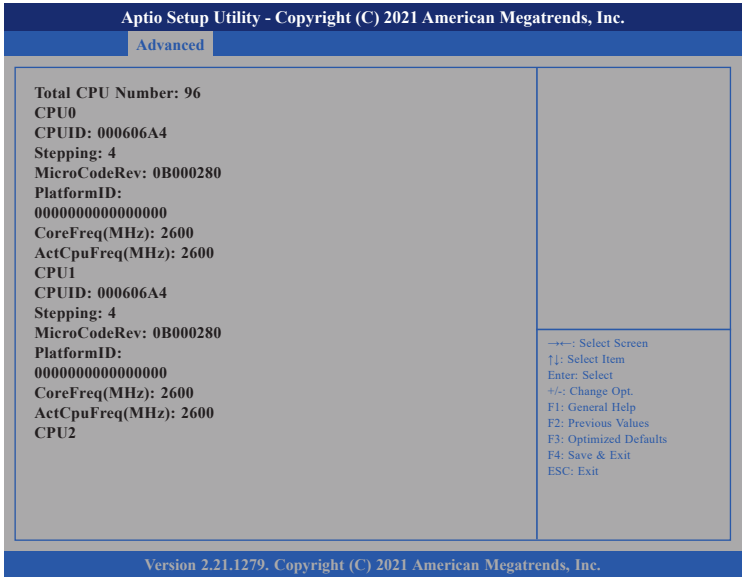
NVMe Configuration

This section is used to display information on the NVMe devices installed.



All Cpu Information

This section is used to display information on the CPU installed.



Platform Configuration

PCH Configuration
Enters the PCH Configuration submenu.

Server ME Configuration
Enters the Server ME Configuration submenu.

PCH Configuration

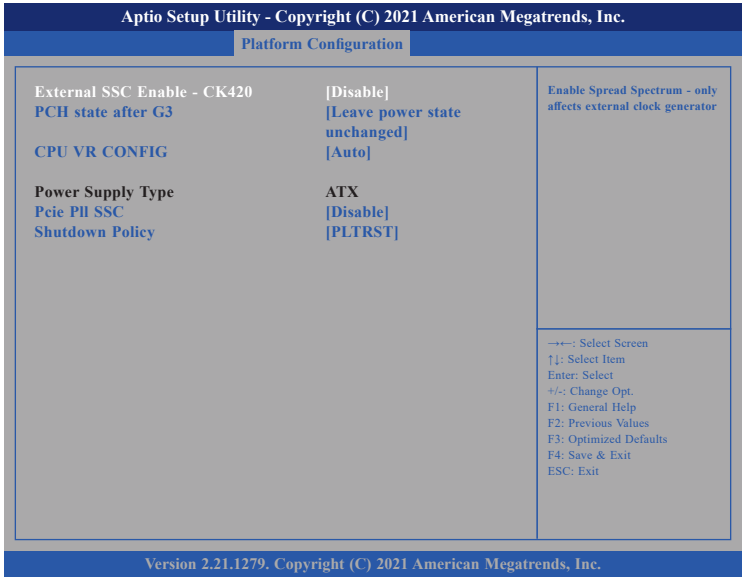
PCH Devices
Enters the PCH Devices submenu.

PCI Express Configuration
Enters the PCI Express Configuration submenu.

PCH SATA/sSATA Configuration
Enters the PCH SATA/sSATA Configuration submenu.

USB Configuration
Enters the USB Configuration submenu.

PCH Devices



External SSC Enable - CK420
Enables or disables spread spectrum clock. Only affects external clock generator.

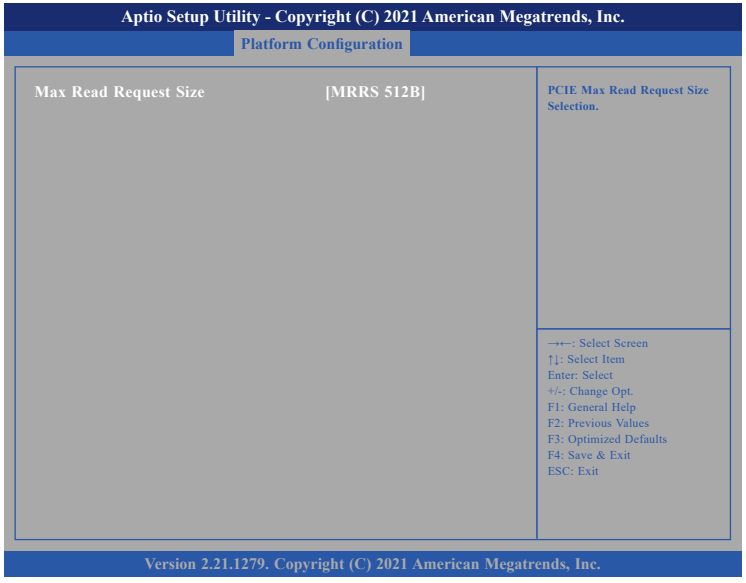
PCH state after G3
Configures the PCH state after G3.

CPU VR CONFIG
Enables or disables CPU VR Config.

Pcie Pll SSC
Enables or disables PCIe Phase Locked Loop for spread spectrum clock.

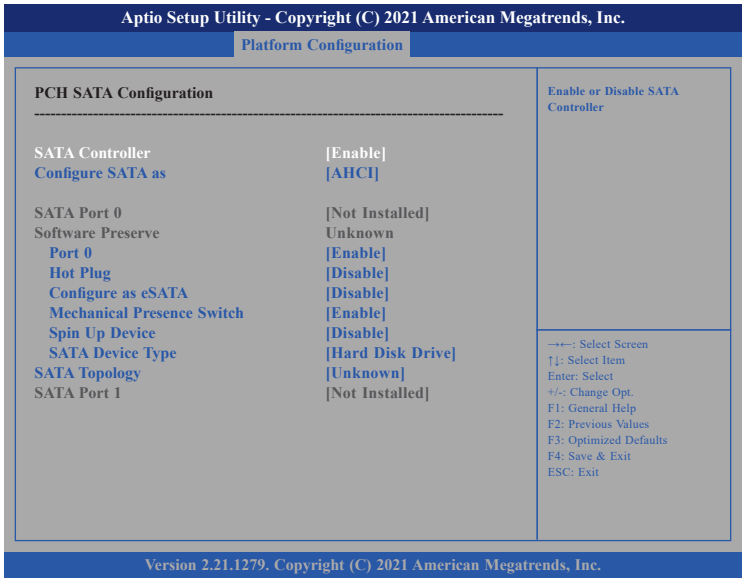
Shutdown Policy
Configures the shutdown policy.

PCI Express Configuration



Max Read Request Size
Configures the PCIe max read request size.

PCH SATA Configuration



SATA Controller(s)
Enables or disables the SATA controller.

Configure SATA as
Configures the SATA mode.

AHCI This option configures the Serial ATA drives to use AHCI (Advanced Host Controller Interface). AHCI allows the storage driver to enable the advanced Serial ATA features which will increase storage performance.

Port 0
Enables or disables SATA port 0.

Hot Plug
Enables or disables hot plugging feature on SATA port 0.

Configure as eSATA
Enables or disables the external SATA option on SATA port 0.

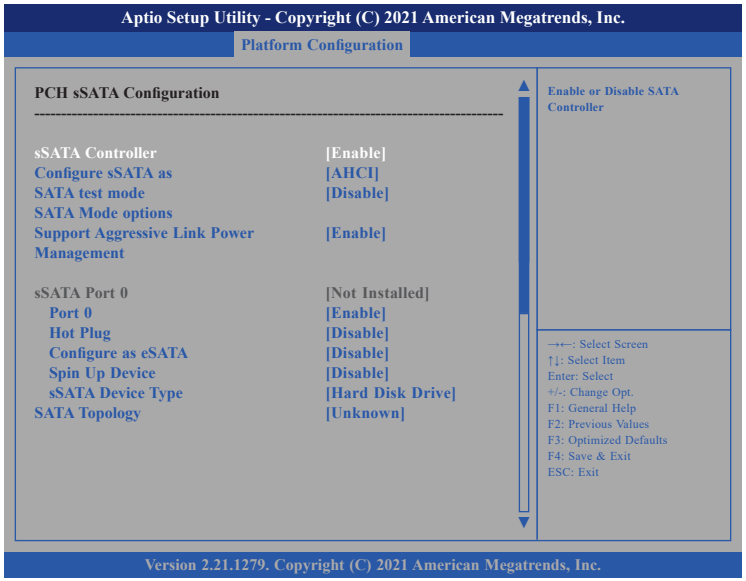
Mechanical Presence Switch
Enables or disables reporting of whether port 0 has a mechanical presence switch. Note: Requires hardware support.

Spin Up Device
Enables or disables staggered spin up on devices connected to SATA port 0 and port 1.

SATA Device Type
Identifies what type of SATA device is connected.

SATA Topology
Identifies what type of SATA connection is used.

PCH sSATA Configuration



sSATA Controller(s)
Enables or disables the SATA controller.

Configure sSATA as
Configures the SATA mode.

AHCI This option configures the Serial ATA drives to use AHCI (Advanced Host Controller Interface). AHCI allows the storage driver to enable the advanced Serial ATA features which will increase storage performance.

SATA Test Mode
Enables or disables SATA test mode.

Support Aggressive Link Power Management
Enables or disables PCH to aggressively enter link power state.

Port 0
Enables or disables SATA port 0.

Hot Plug
Enables or disables hot plugging feature on SATA port 0.

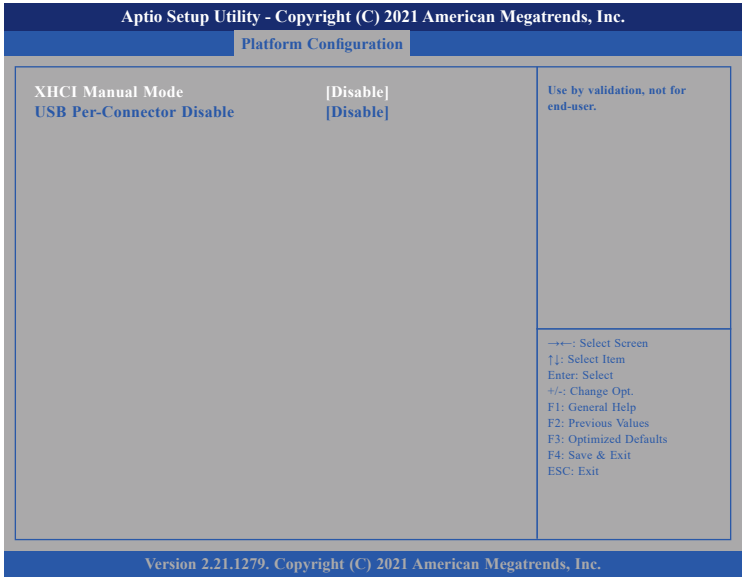
Configure as eSATA
Enables or disables the external SATA option on SATA port 0.

Spin Up Device
Enables or disables staggered spin up on devices connected to SATA port 0 and port 1.

sSATA Device Type
Identifies what type of SATA device is connected.

SATA Topology
Identifies what type of SATA connection is used.

USB Configuration (PCH)



XHCI Manual Mode

Enables or disables XHCI manual mode.

USB Per-Connector Disable

Provides the option to enable or disable each USB connector.

Server ME Configuration

Displays information of the firmware installed in the system.

Socket Configuration

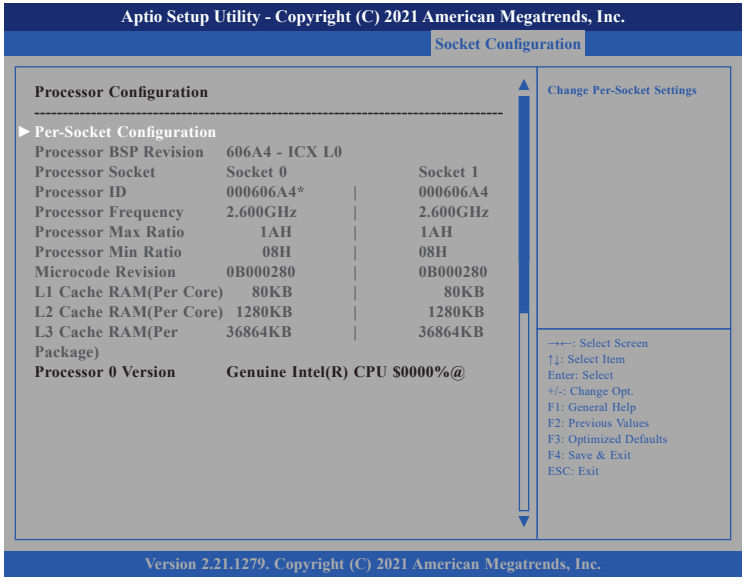
Processor Configuration
Enters the Processor Configuration submenu.

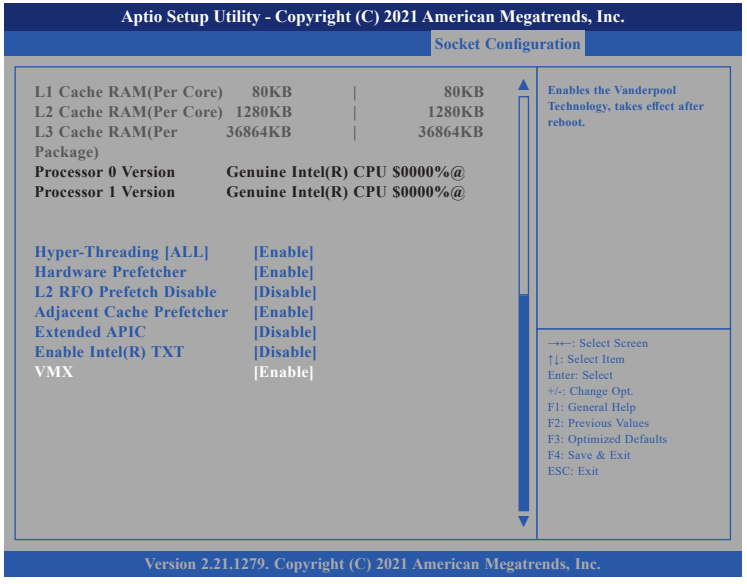
Common RefCode Configuration
Enters the Common RefCode Configuration submenu.

UPI Configuration and Memory Configuration
Enters the UPI Configuration and Memory Configuration submenu.

IIO Configuration and Advanced Power Management Configuration
Enters the IIO Configuration and Advanced Power Management Configuration submenu.

Processor Configuration





Hyper-Threading [ALL]
Enables or disables hyper-threading technology.

Hardware Prefetcher
Enables or disables the MLC streamer prefetcher.

L2 RFO Prefetch Disable
Enables or disables L2 RFO prefetch.

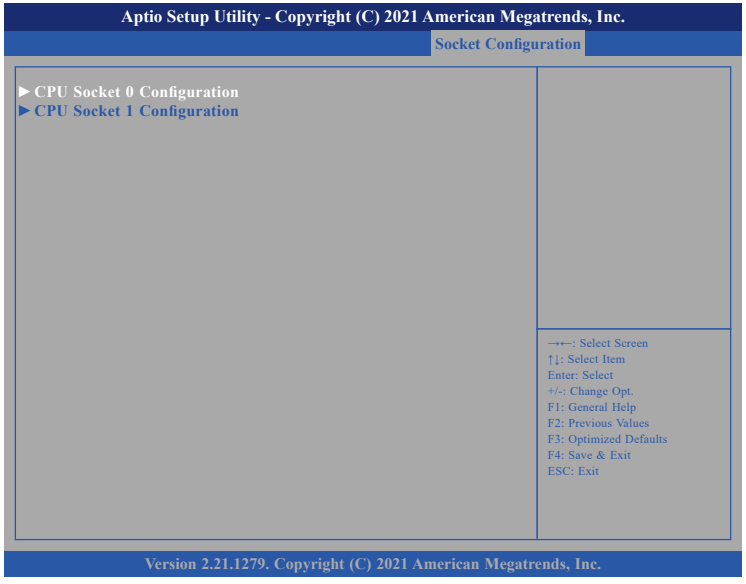
Adjacent Cache Prefetcher
Enables or disables prefetching of adjacent cache lines.

Extended APIC
Enables or disables extended APIC support.

Enable Intel® TXT
Enables or disables Intel TXT support.

VMX
Enables or disables Virtual Machine Extensions.

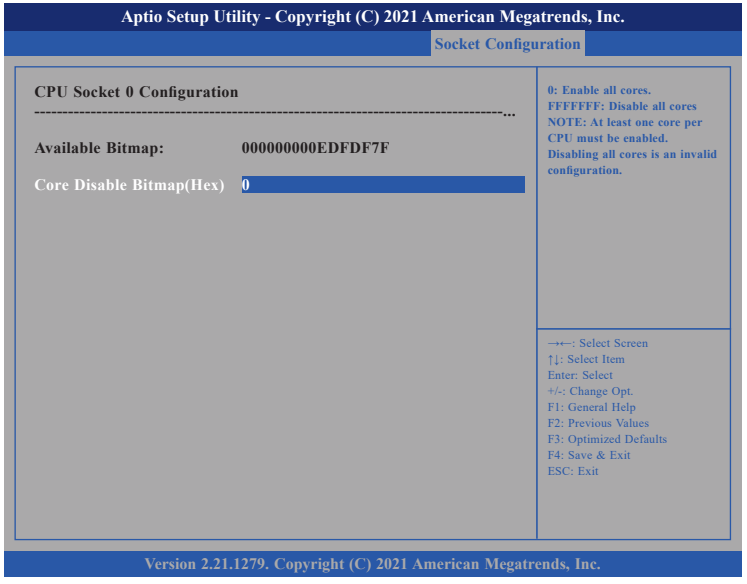
Per-Socket Configuration



CPU Socket 0 Configuration
Processor settings for the CPU on socket 0.

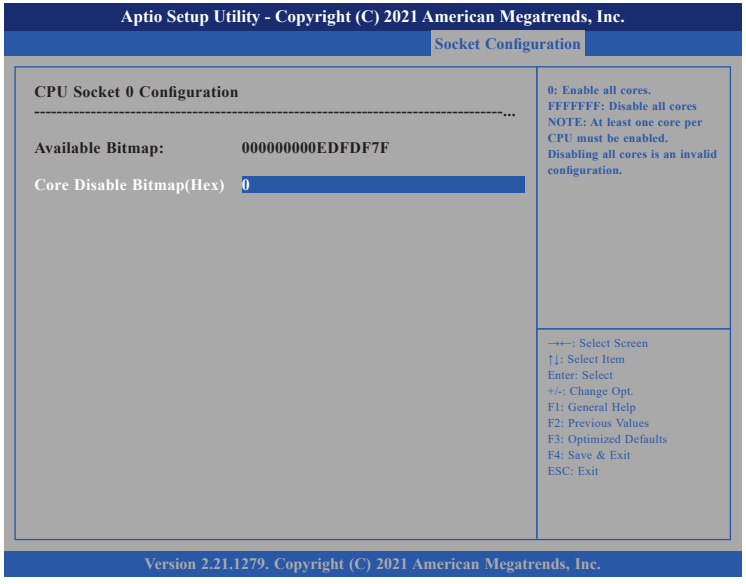
CPU Socket 1 Configuration
Processor settings for the CPU on socket 1.

CPU Socket 0 Configuration



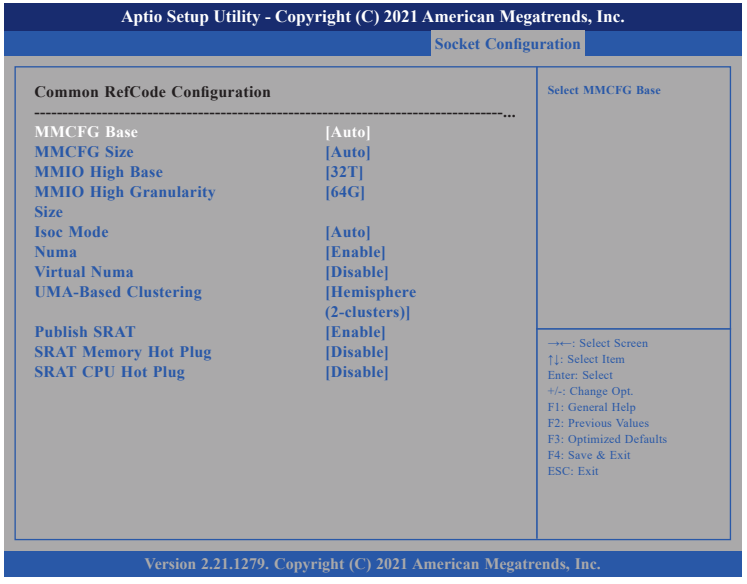
Cores Disable Bitmap
Provides the option to enable or disable all cores. 0 means enable all cores. FFFFFFF means disable all cores.

CPU Socket 0 Configuration



Cores Disable Bitmap
Provides the option to enable or disable all cores. 0 means enable all cores. FFFFFFF means disable all cores.

Common RefCode Configuration



MMCFG Base
Configures the memory mapped configuration (MMCFG) base address.

MMCFG Size
Configures the MMCFG size.

MMIO High Base
Configures the base memory size of MMIO high base.

MMIO High Granularity Size
Configures the high memory size of MMIO high base.

Isoc Mode
Enables or disables Isochronous support.

Numa
Enables or disables Non-Uniform Memory Access support.

Virtual Numa
Enables or disables Virtual Numa support.

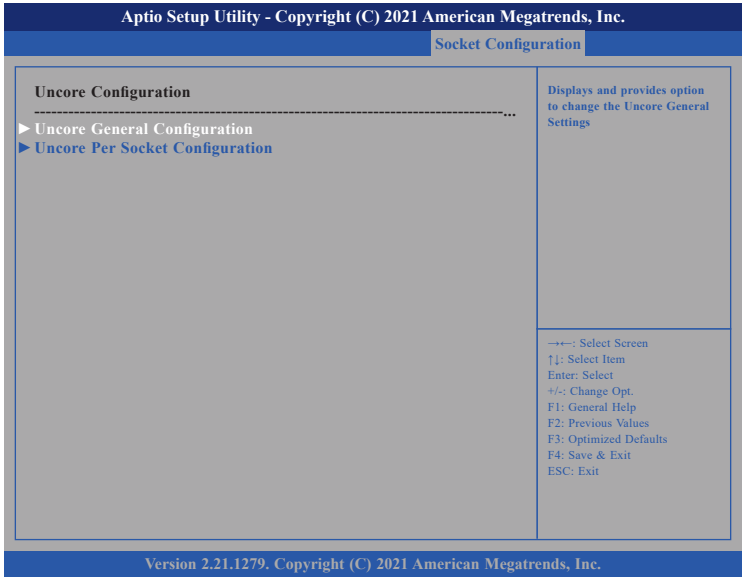
UMA-Based Clustering
Configures the option for UMA-Based Clustering

Publish SRAT
Enables or disables SRAT (Static Resource Affinity Table).

SRAT Memory Hot Plug
Enables or disables SRAT Memory Hot-Plugging.

SRAT CPU Hot Plug
Enables or disables SRAT CPU Hot-Plugging.

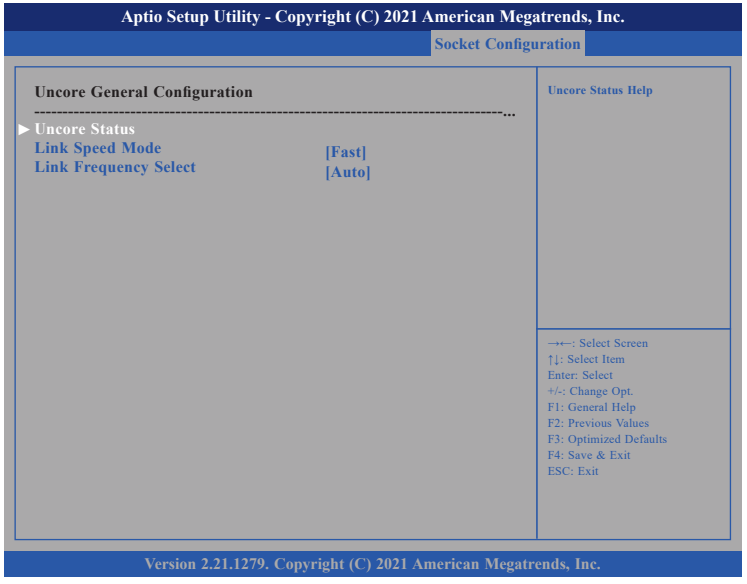
Uncore Configuration



Uncore General Configuration
Enters the Uncore General Configuration submenu.

Uncore Per Socket Configuration
Enters the Uncore Per Socket Configuration submenu.

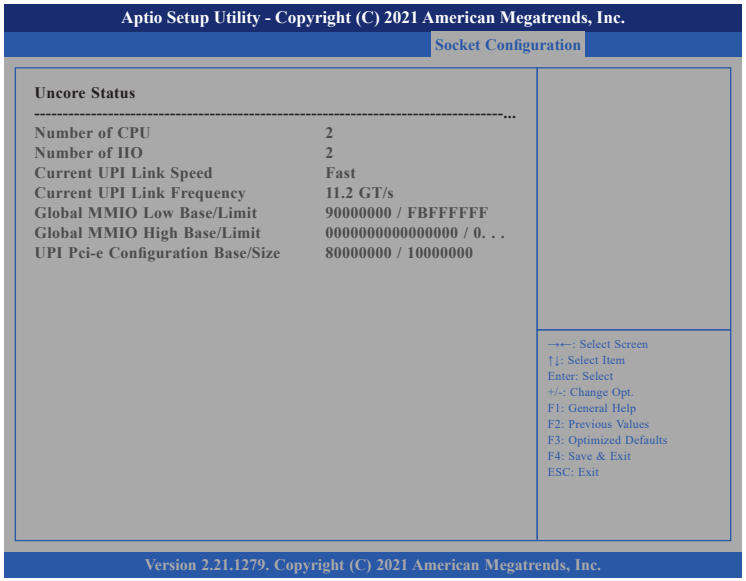
Uncore General Configuration



Link Speed Mode
Configures the link speed mode.

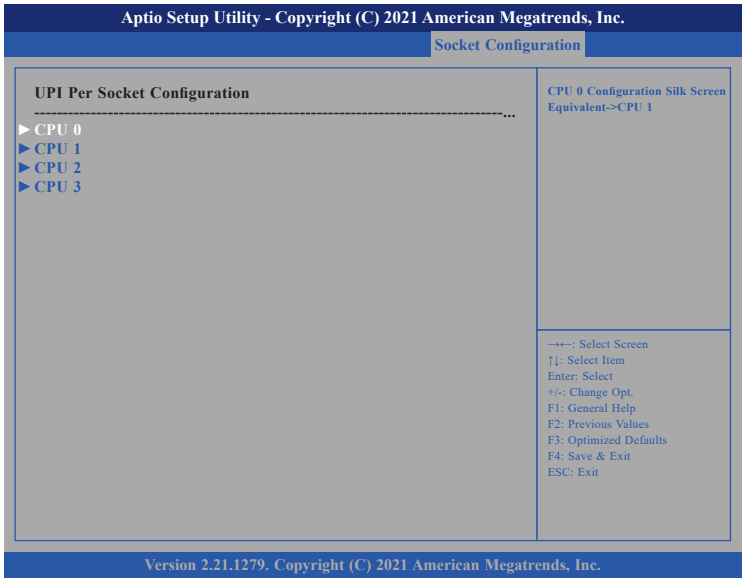
Link Frequency Select
Configures the uncore frequency.

Uncore Status



Displays information on the current uncore configuration.

UPI Per Socket Configuration



CPU 0
Enters the CPU 0 submenu.

CPU 1
Enters the CPU 1 submenu.

CPU 2
Enters the CPU 1 submenu.

CPU 3
Enters the CPU 1 submenu.

Uncore Per Socket Configuration CPU 0

CPU 0 UPI Port 0
Enters the CPU 0 UPI Port 0 configuration submenu.

CPU 0 UPI Port 1
Enters the CPU 0 UPI Port 1 configuration submenu.

CPU 0 UPI Port 2
Enters the CPU 0 UPI Port 2 configuration submenu.

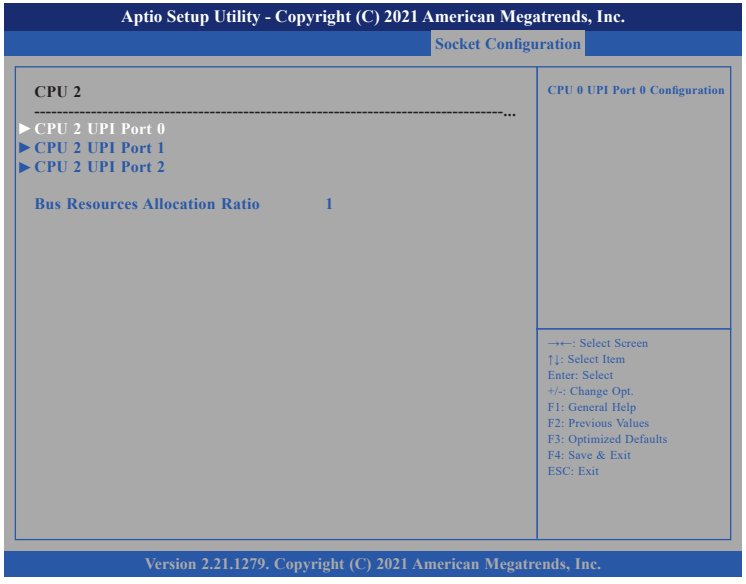
Uncore Per Socket Configuration CPU 1

CPU 1 UPI Port 0
Enters the CPU 1 UPI Port 0 configuration submenu.

CPU 1 UPI Port 1
Enters the CPU 1 UPI Port 1 configuration submenu.

CPU 1 UPI Port 2
Enters the CPU 1 UPI Port 2 configuration submenu.

Uncore Per Socket Configuration CPU 2



CPU 2 UPI Port 0
Enters the CPU 2 UPI Port 0 configuration submenu.

CPU 2 UPI Port 1
Enters the CPU 2 UPI Port 1 configuration submenu.

CPU 2 UPI Port 2
Enters the CPU 2 UPI Port 2 configuration submenu.

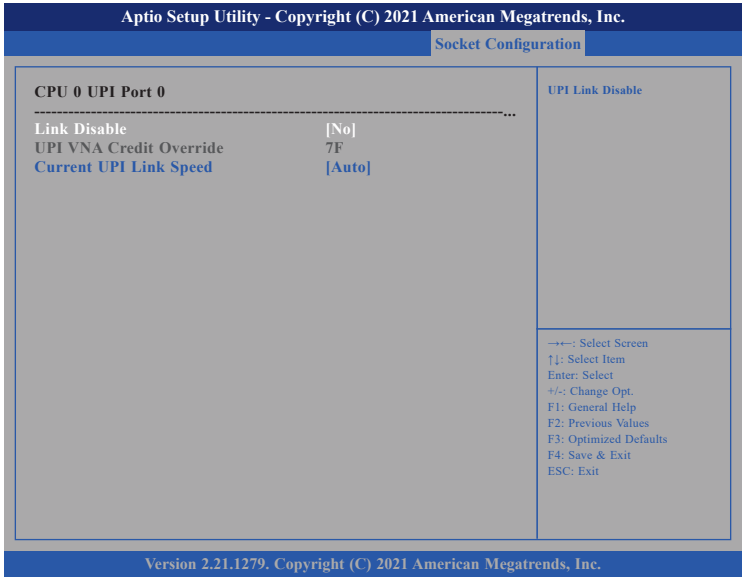
Uncore Per Socket Configuration CPU 3

CPU 3 UPI Port 0
Enters the CPU 3 UPI Port 0 configuration submenu.

CPU 3 UPI Port 1
Enters the CPU 3 UPI Port 1 configuration submenu.

CPU 3 UPI Port 2
Enters the CPU 3 UPI Port 2 configuration submenu.

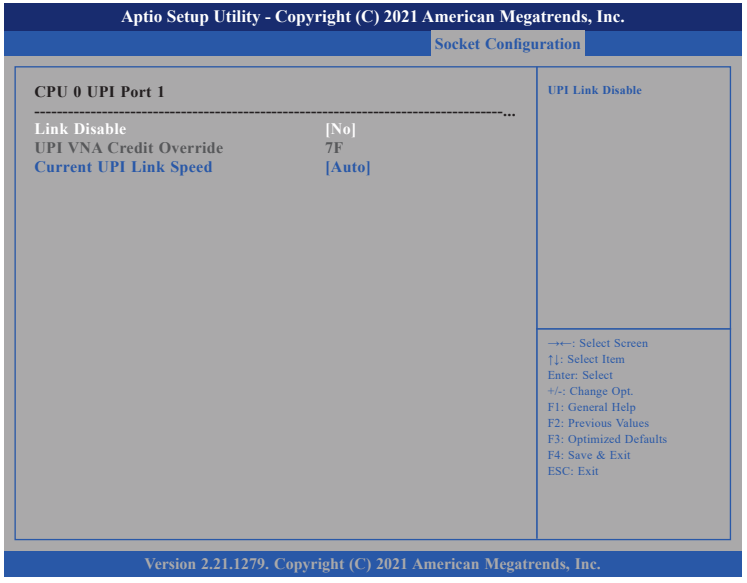
CPU 0 UPI Port 0



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

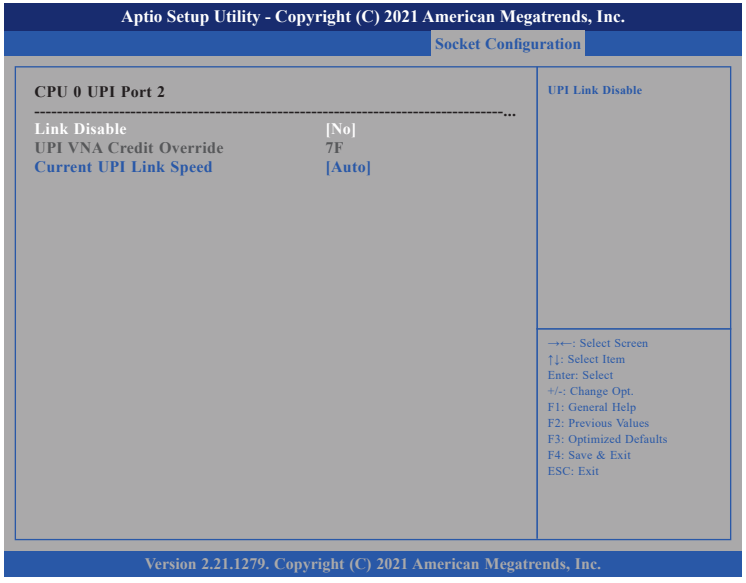
CPU 0 UPI Port 1



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

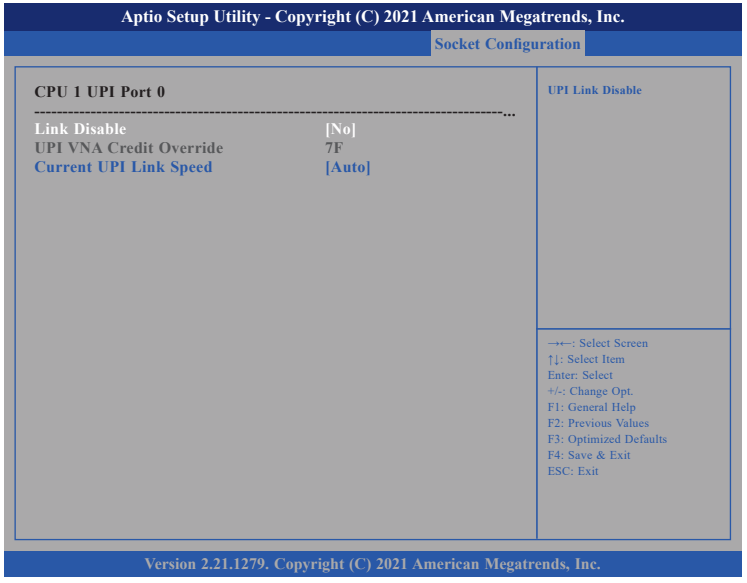
CPU 0 UPI Port 2



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

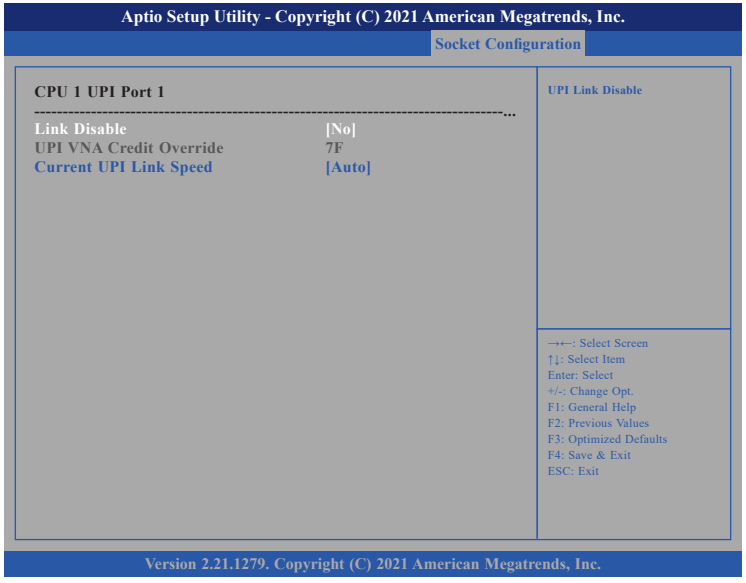
CPU 1 UPI Port 0



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

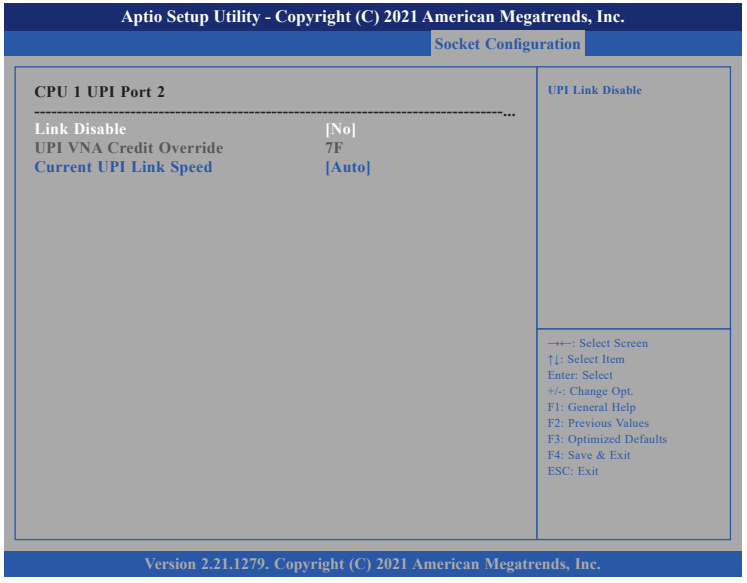
CPU 1 UPI Port 1



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

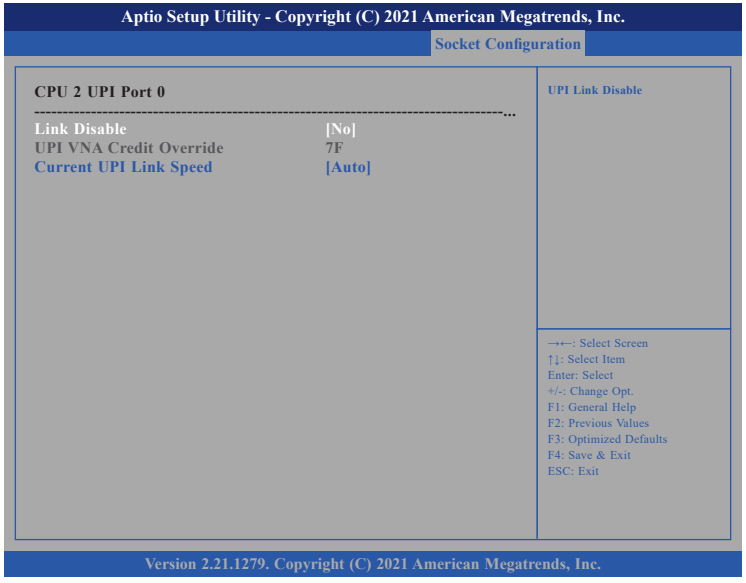
CPU 1 UPI Port 2



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

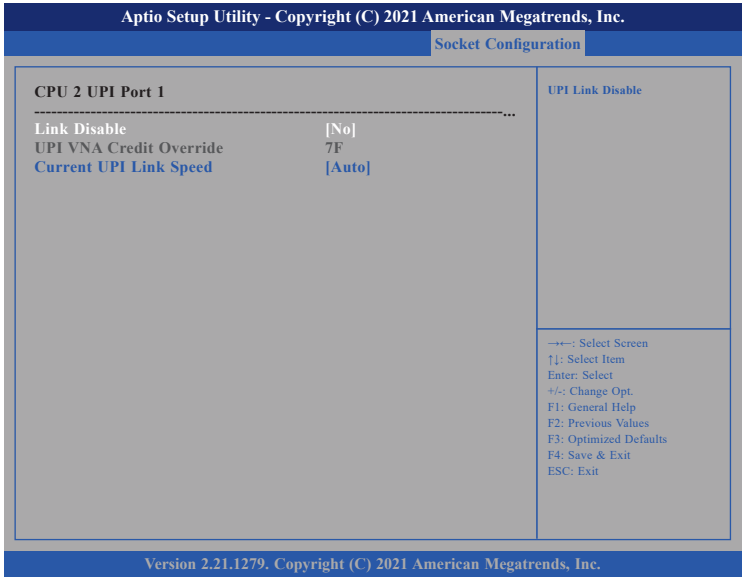
CPU 2 UPI Port 0



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

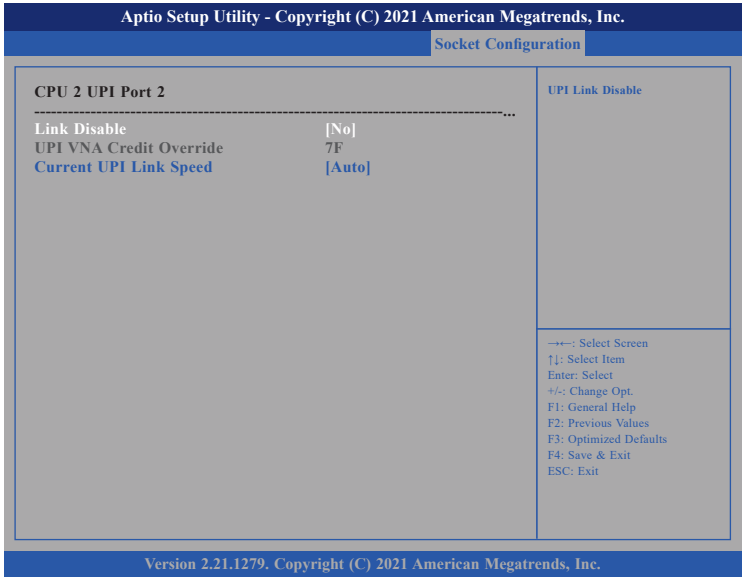
CPU 2 UPI Port 1



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

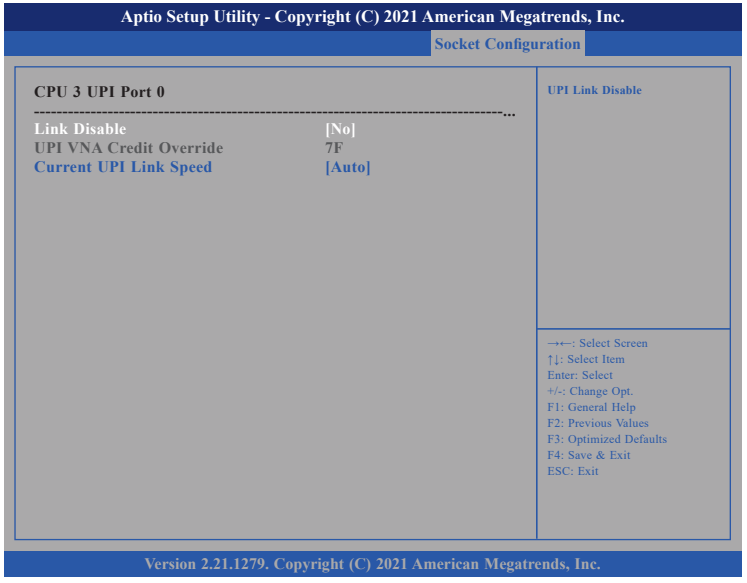
CPU 2 UPI Port 2



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

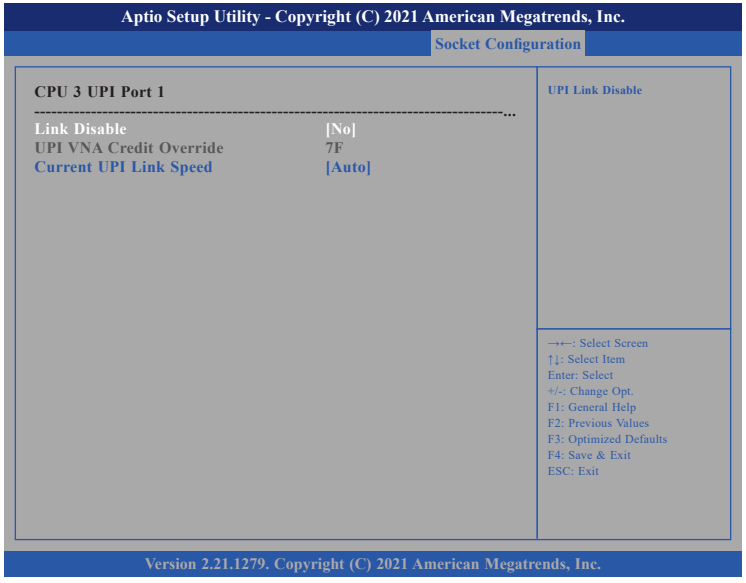
CPU 3 UPI Port 0



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

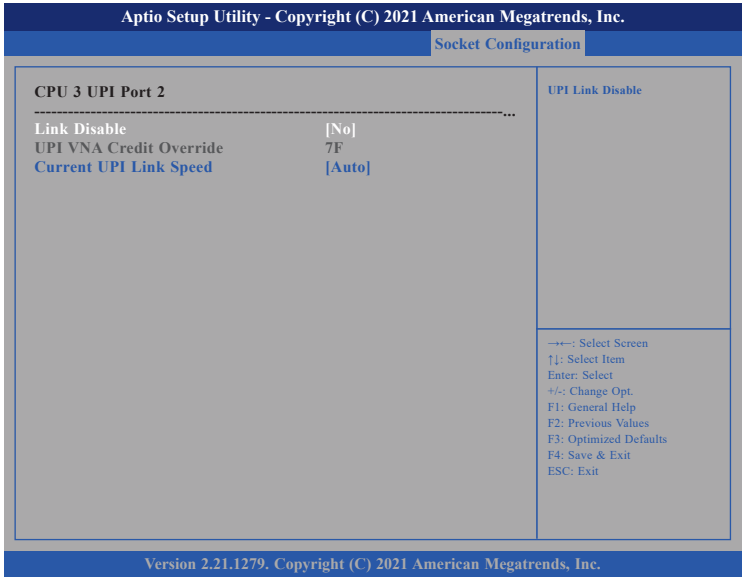
CPU 3 UPI Port 1



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

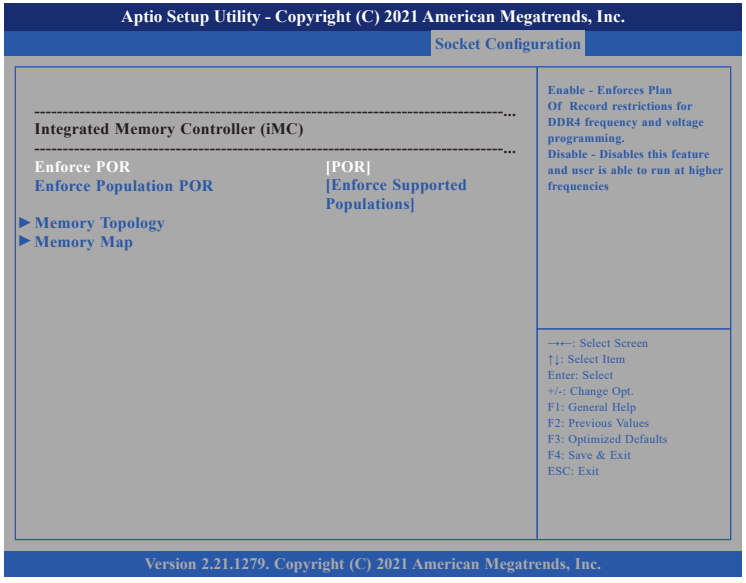
CPU 3 UPI Port 2



Link Disable
Enables or disables the UPI link.

Current UPI Link Speed
Configures the current UPI link speed.

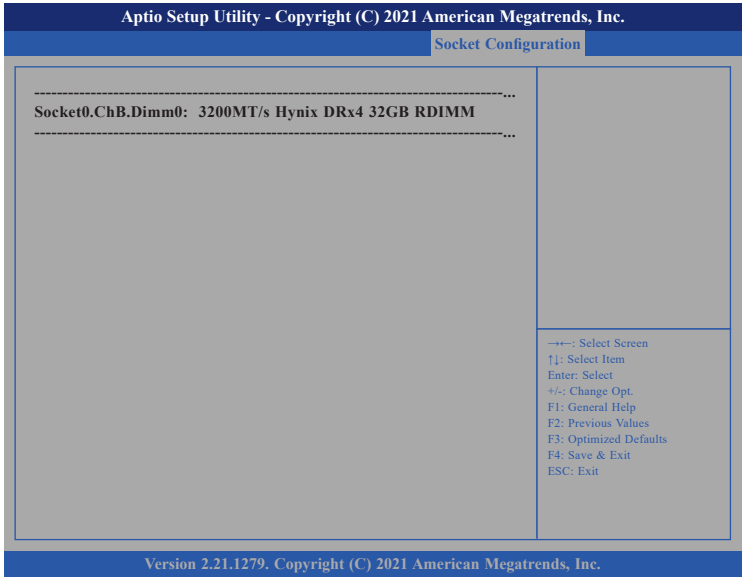
Memory Configuration



Enforce POR
Configures the options for Enforce Plan of Record. When enabled, Plan of Record restrictions for DDR4 frequency and voltage programming is enforced.

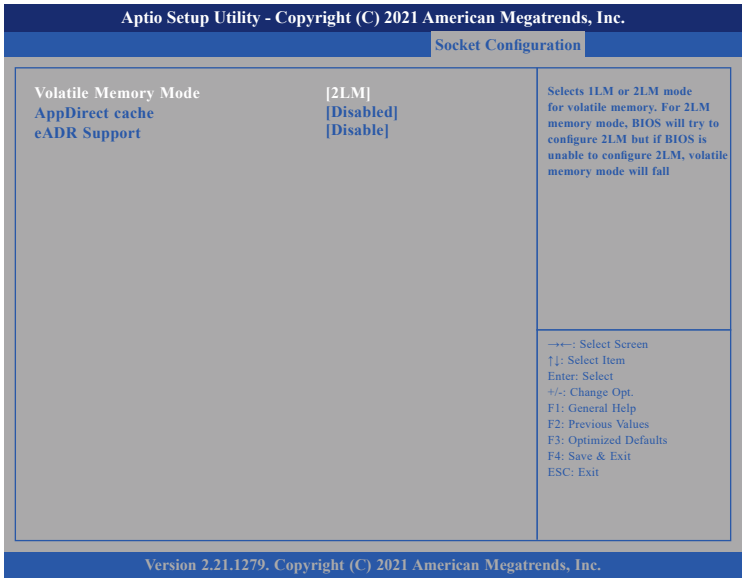
Enforce Population POR
Enables or disables Enforce Population POR.

Memory Topology



Detects and displays the information on the memory installed.

Memory Map

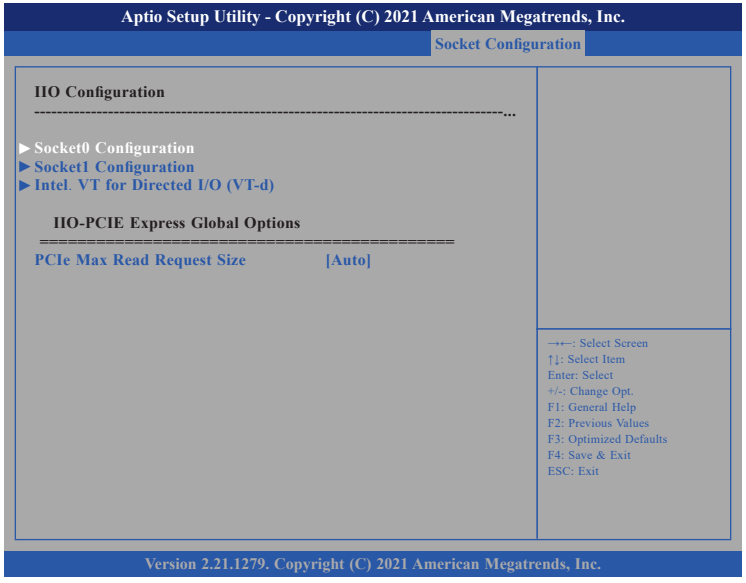


Volatile Memory Mode
Configures 1LM or 2LM mode for volatile memory. For 2LM memory mode, BIOS will try to configure 2LM but if BIOS is unable to configure 2LM, volatile memory mode will fall.

AppDirect cache
Enables or disables AppDirect cache.

eADR Support
Enables or disables eADR support.

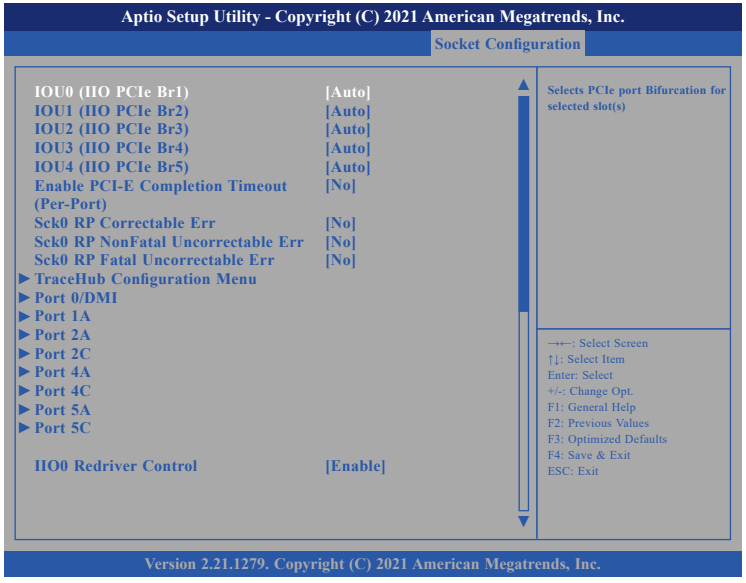
IIO Configuration



Socket0 Configuration and Socket1 Configuration
Enters the Socket0 and Socket1 Configuration submenu.

Intel. VT for Directed I/O (VT-d)
Enters the Intel® VT for Directed I/O (VT-d) submenu.

Socket0 Configuration



IOU0 (IIO PCIe Br1) to IOU4 (IIO PCIe Br5)
Port Bifurcation settings for IOU 0 to IOU 4.

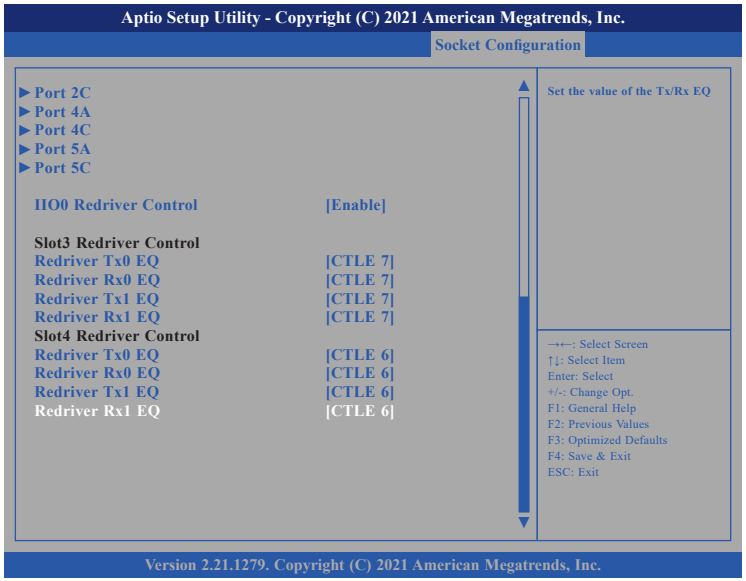
Enable PCI-E Completion Timeout (Per-Port)
Enables or disables PCI-E completion timeout.

Sck0 RP Correctable Err
Enables or disables correctable error interruption.

Sck0 RP NonFatal Uncorrectable Err
Enables or disables non-fatal error interruption.

Sck0 RP Fatal Uncorrectable Err
Enable or disables fatal error interruption.

Socket0 Configuration

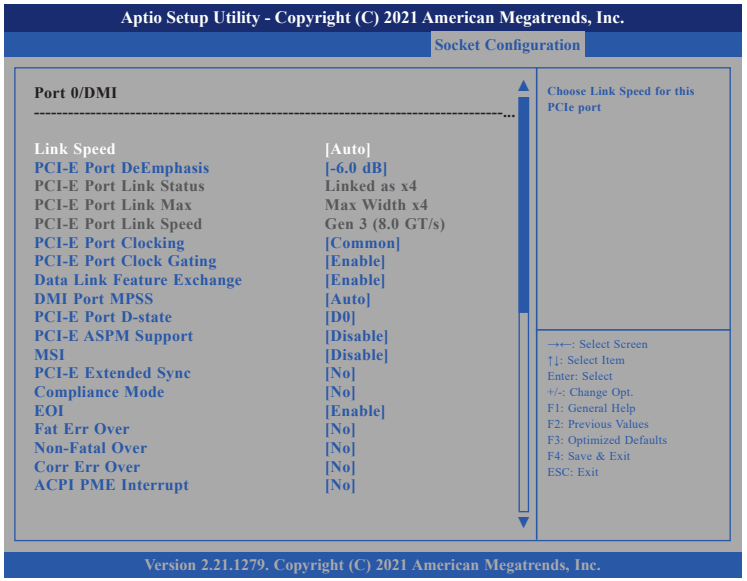


IIO0 Redriver Control
Configures the redriver options for IIO0.

Slot7 Redriver Control
Configures the value of the Tx/Rx EQ for slot 3.

Slot8 Redriver Control
Configures the value of the Tx/Rx EQ for slot 4.

Port 0/DMI



Link Speed
Configures the link speed for the PCIe port.

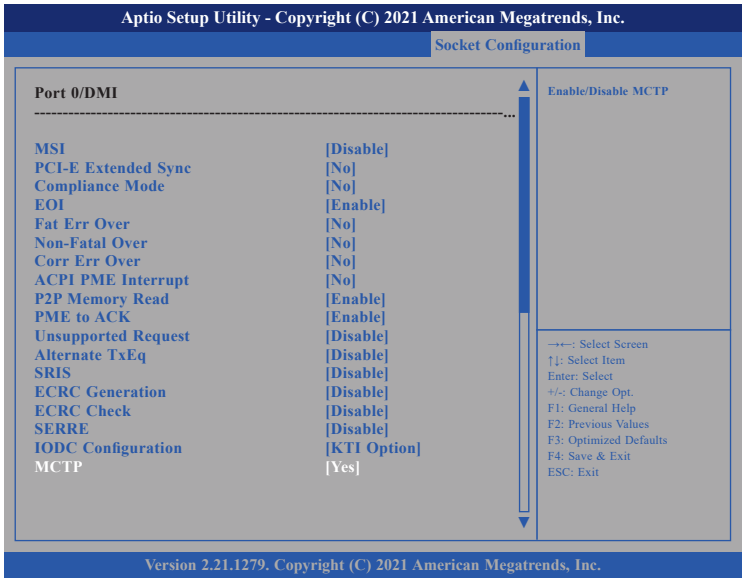
PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

Port 0/DMI



DMI Port MPSS
Configures the option for max payload size supported.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

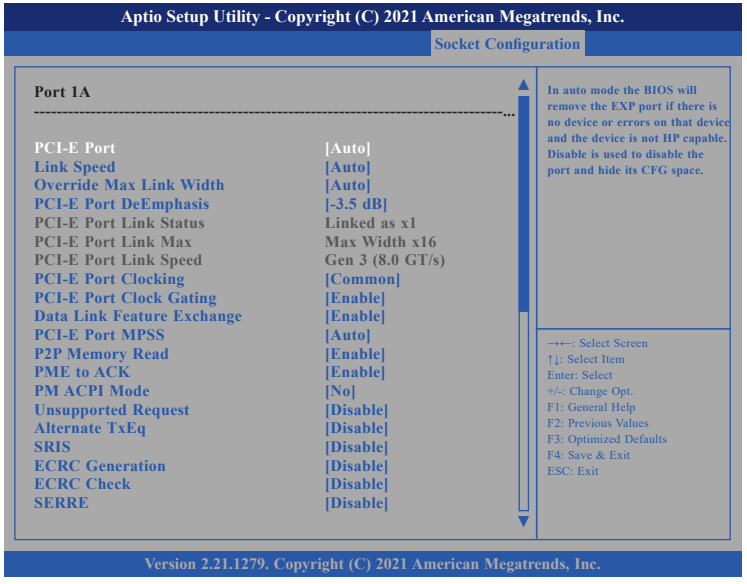
ECRC Check
Enables or disables ECRC Checking.

SERRE
Enables or disables SERRE bit.

IODC Configuration
Configures the option for IODC (IO Direct Cache).

MCTP
Enables or disables MCTP.

Port 1A



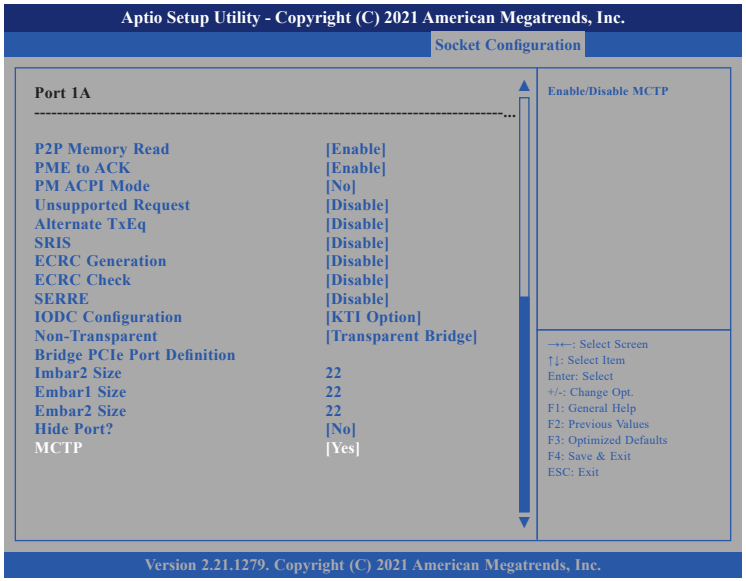
PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

Port 1A



PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

SERRE
Enables or disables SERRE bit.

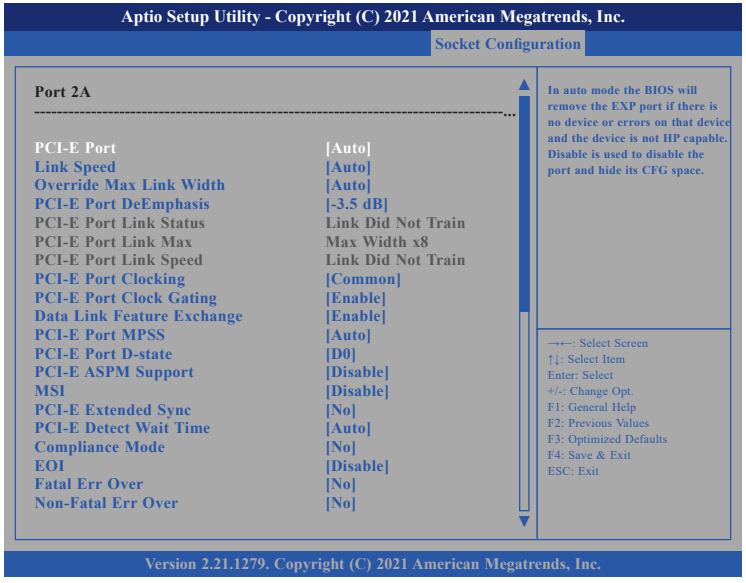
IODC Configuration
Configures the option for IODC (IO Direct Cache).

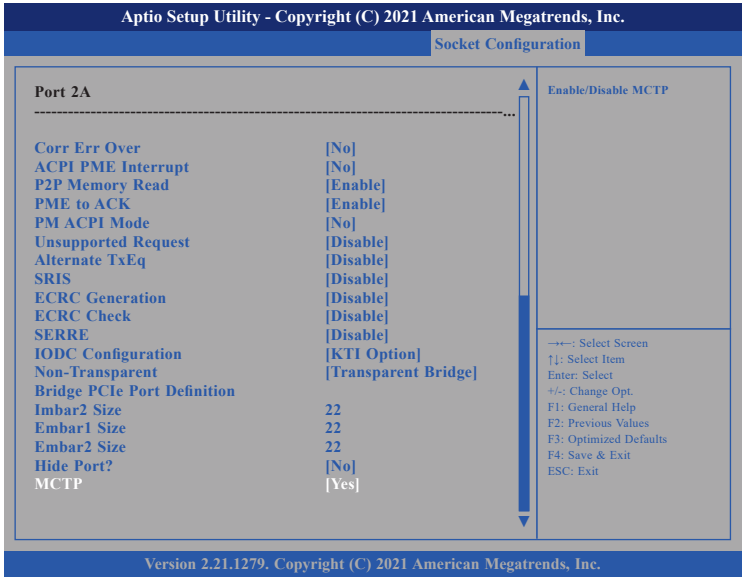
Non-Transparent Bridge PCIe Port Definition
Configures the option for the PCIe port.

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP.

Port 2A





PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

SERRE
Enables or disables SERRE bit.

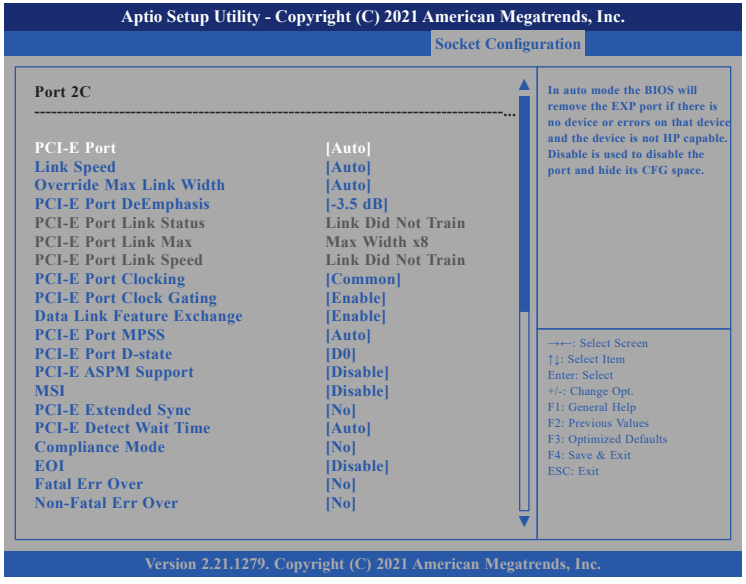
IODC Configuration
Configures the option for IODC (IO Direct Cache).

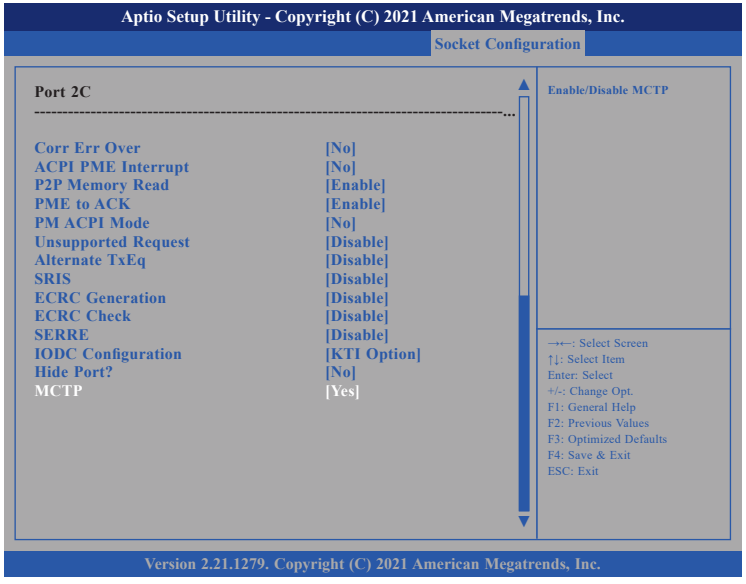
Non-Transparent Bridge PCIe Port Definition
Configures the option for the PCIe port.

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Port 2C





PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

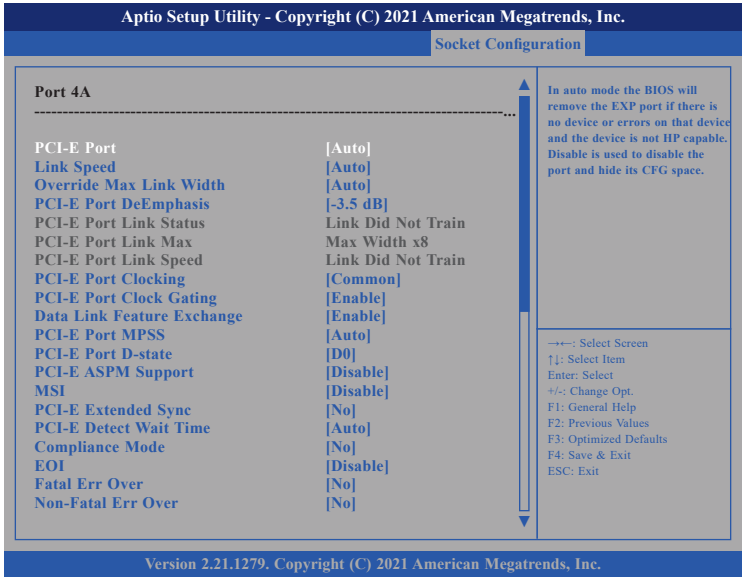
SERRE
Enables or disables SERRE bit.

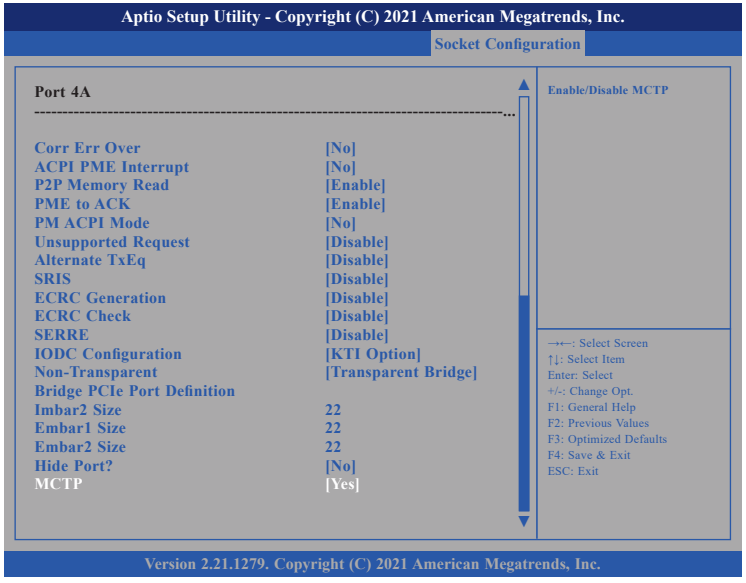
IODC Configuration
Configures the option for IODC (IO Direct Cache).

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Port 4A





PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

SERRE
Enables or disables SERRE bit.

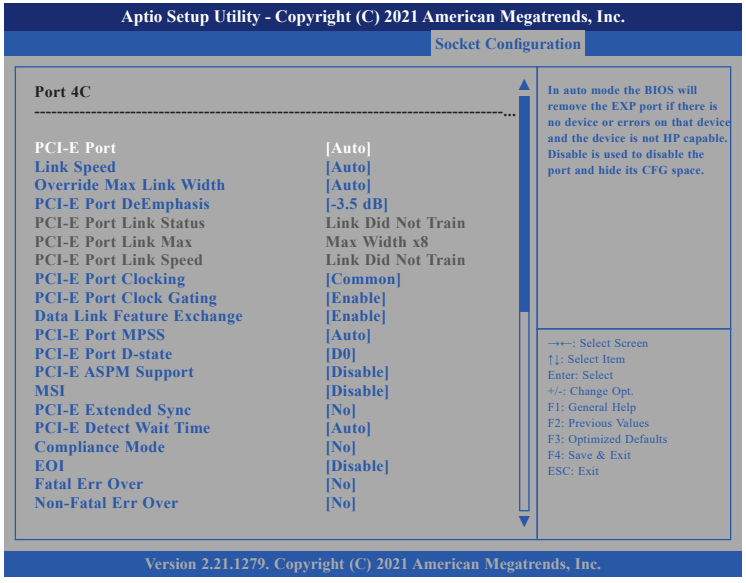
IODC Configuration
Configures the option for IODC (IO Direct Cache).

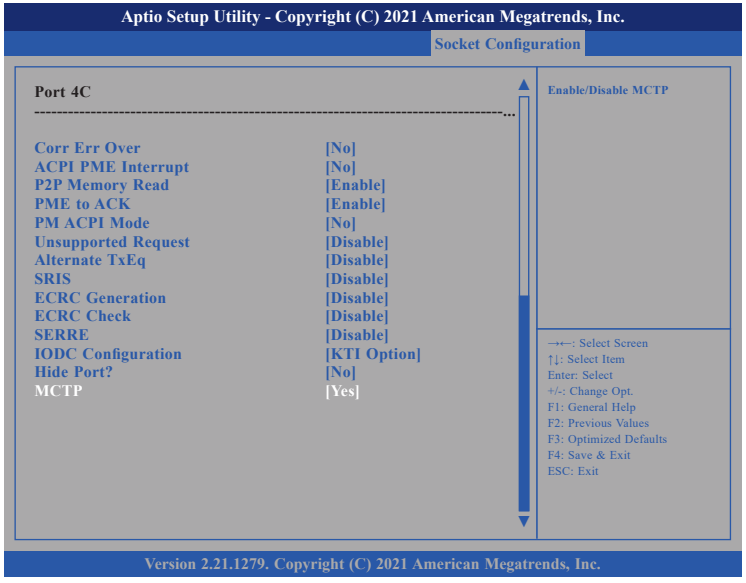
Non-Transparent Bridge PCIe Port Definition
Configures the option for the PCIe port.

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Port 4C





PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

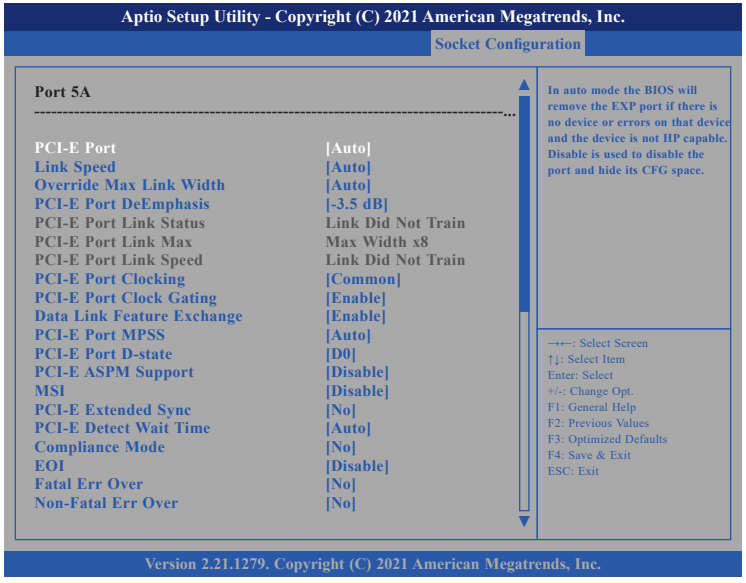
SERRE
Enables or disables SERRE bit.

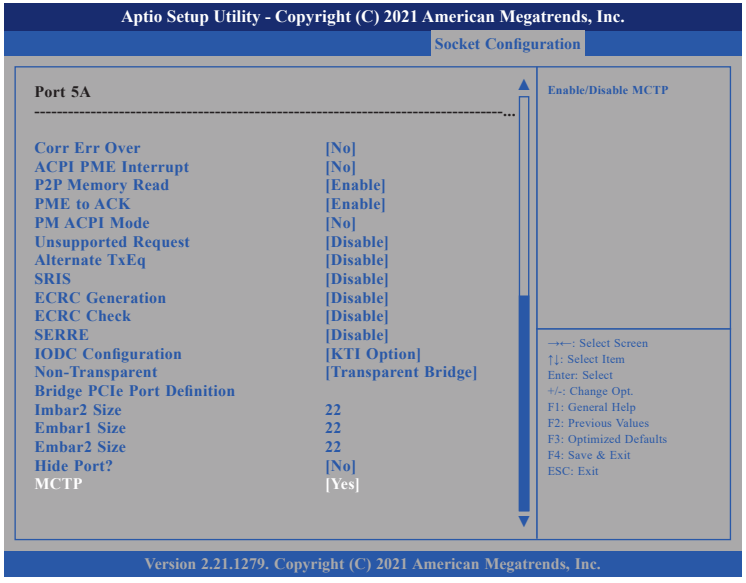
IODC Configuration
Configures the option for IODC (IO Direct Cache).

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Port 5A





PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

SERRE
Enables or disables SERRE bit.

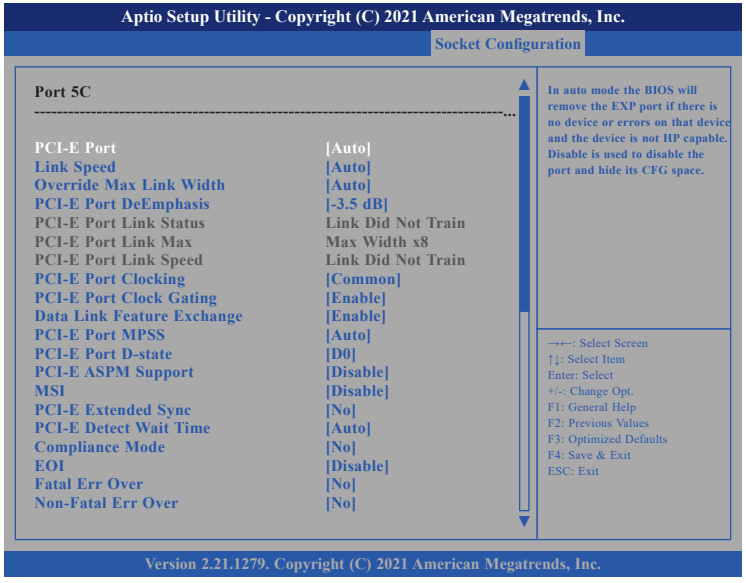
IODC Configuration
Configures the option for IODC (IO Direct Cache).

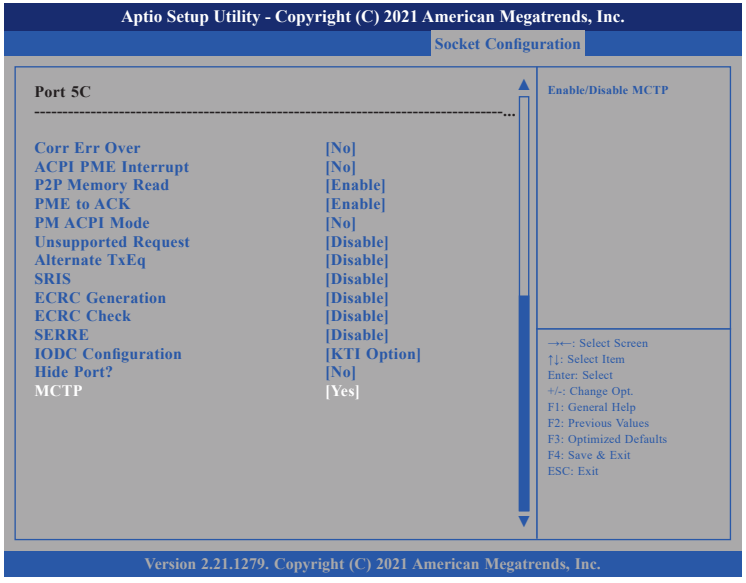
Non-Transparent Bridge PCIe Port Definition
Configures the option for the PCIe port.

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Port 5C





PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

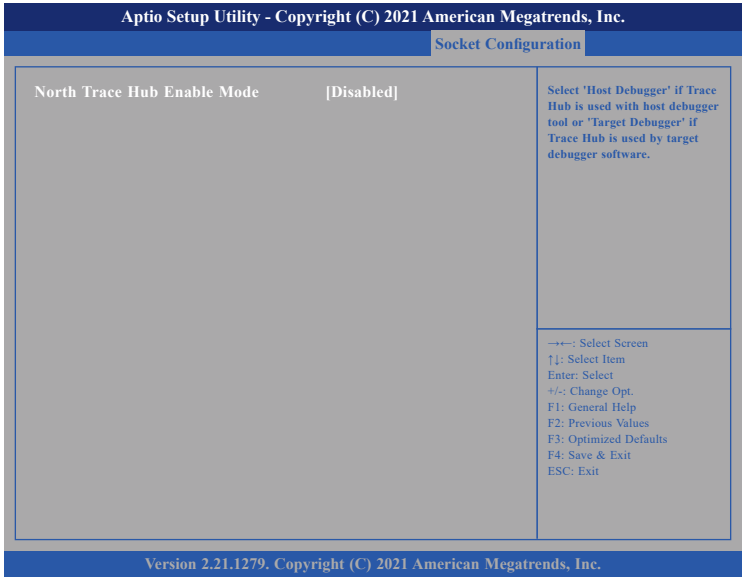
SERRE
Enables or disables SERRE bit.

IODC Configuration
Configures the option for IODC (IO Direct Cache).

Hide Port?
Enables or disables the option to hide the root port.

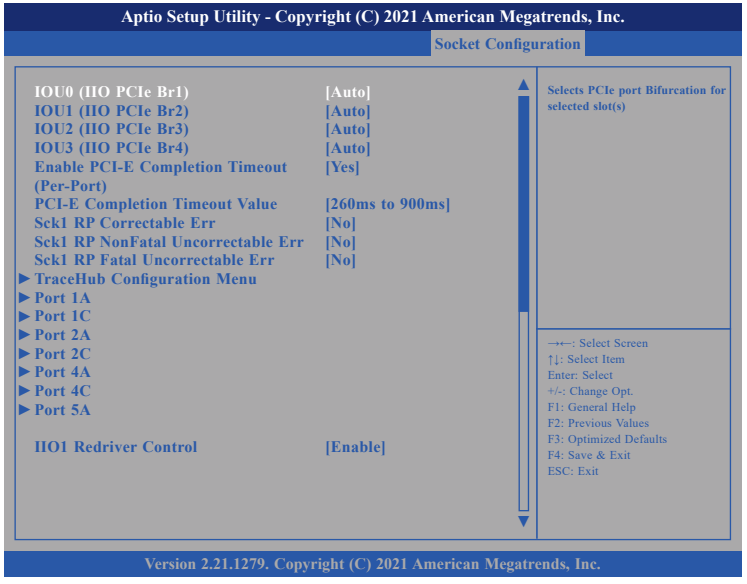
MCTP
Enables or disables MCTP

TraceHub Configuration Menu (Socket 0)



North Trace Hub Enable Mode
Select 'Host Debugger' if Trace Hub is used with host debugger tool or 'Target Debugger' if Trace Hub is used by target debugger software.

Socket1 Configuration



IOU0 (IIO PCIe Br1) to IOU3 (IIO PCIe Br4)
Port Bifurcation settings for IOU 0 to IOU 4.

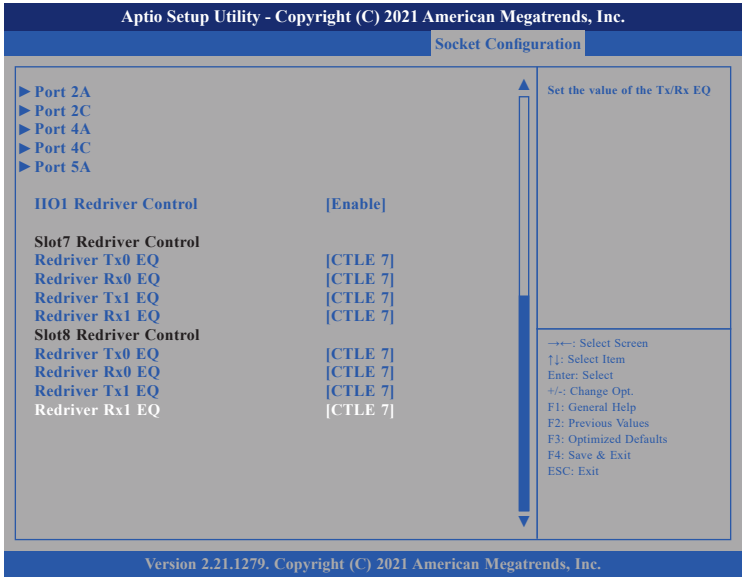
Enable PCI-E Completion Timeout (Per-Port)
Enables or disables PCI-E completion timeout.

PCI-E Completion Timeout Value
Configures the PCI-E completion timeout value.

Sck1 RP Correctable Err
Enables or disables correctable error interruption.

Sck1 RP NonFatal Uncorrectable Err
Enables or disables non-fatal error interruption.

Socket1 Configuration



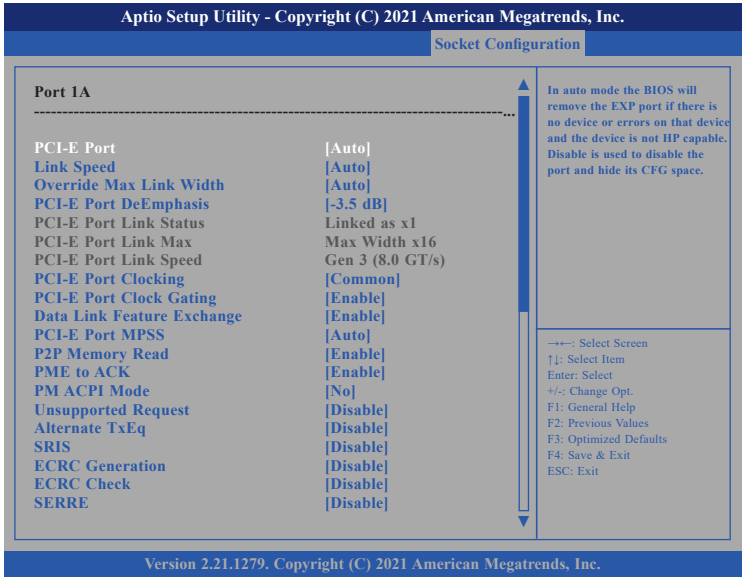
Sck1 RP Fatal Uncorrectable Err
Enable or disables fatal error interruption.

IIO1 Redriver Control
Configures the redriver options for IIO1.

Slot7 Redriver Control
Configures the value of the Tx/Rx EQ for slot 7.

Slot8 Redriver Control
Configures the value of the Tx/Rx EQ for slot 8.

Port 1A



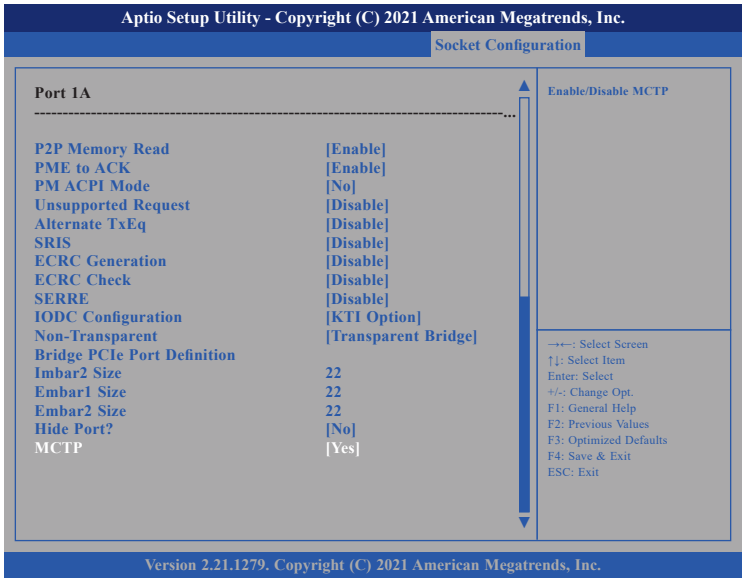
PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

Port 1A



PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

SERRE
Enables or disables SERRE bit.

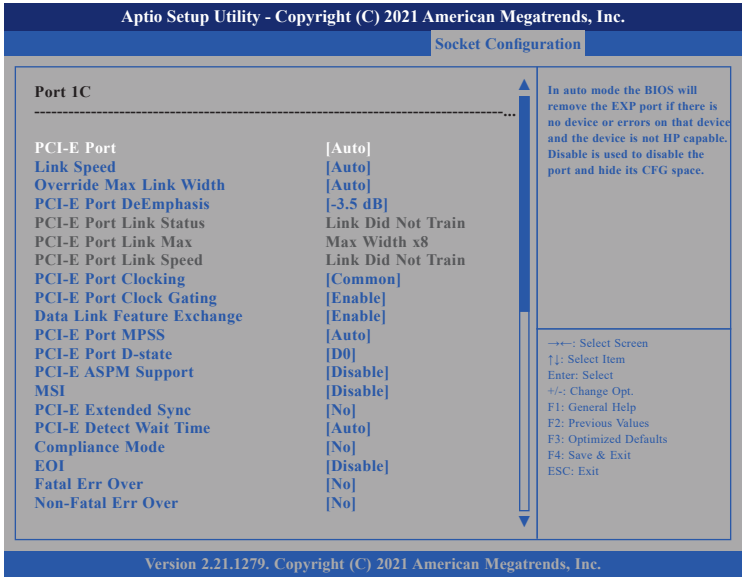
IODC Configuration
Configures the option for IODC (IO Direct Cache).

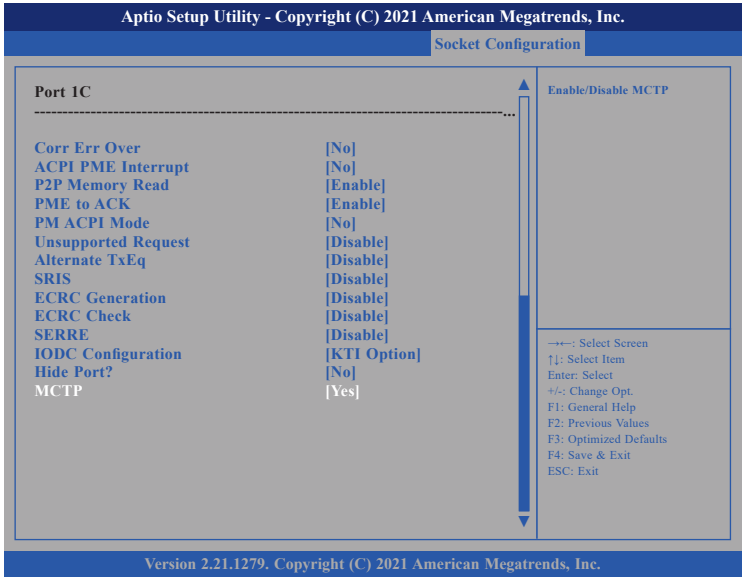
Non-Transparent Bridge PCIe Port Definition
Configures the option for the PCIe port.

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Port 1C





PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

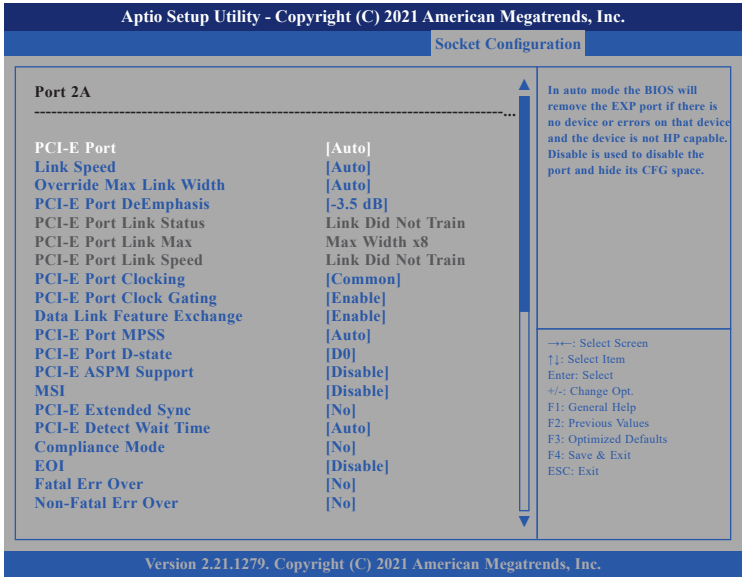
SERRE
Enables or disables SERRE bit.

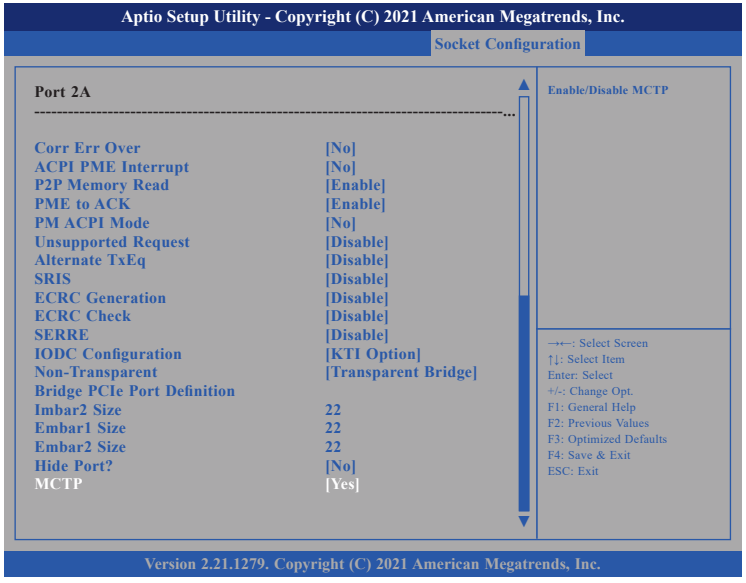
IODC Configuration
Configures the option for IODC (IO Direct Cache).

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Port 2A





PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

SERRE
Enables or disables SERRE bit.

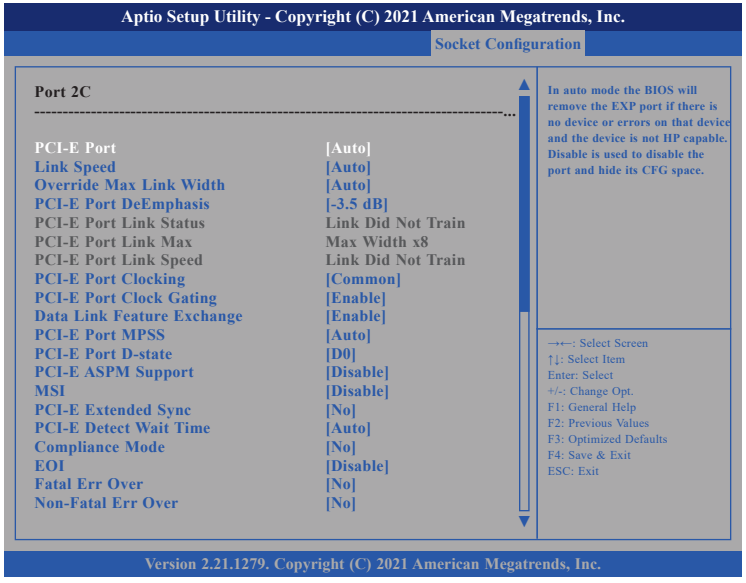
IODC Configuration
Configures the option for IODC (IO Direct Cache).

Non-Transparent Bridge PCIe Port Definition
Configures the option for the PCIe port.

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Port 2C

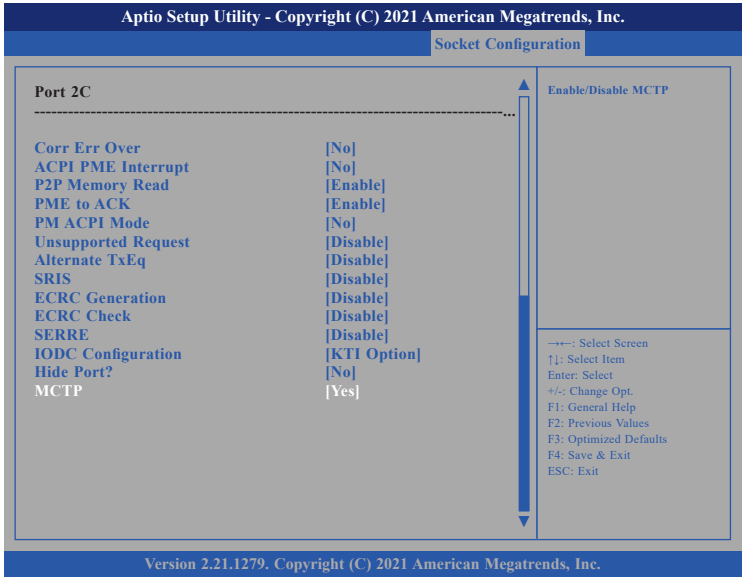


PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.



PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

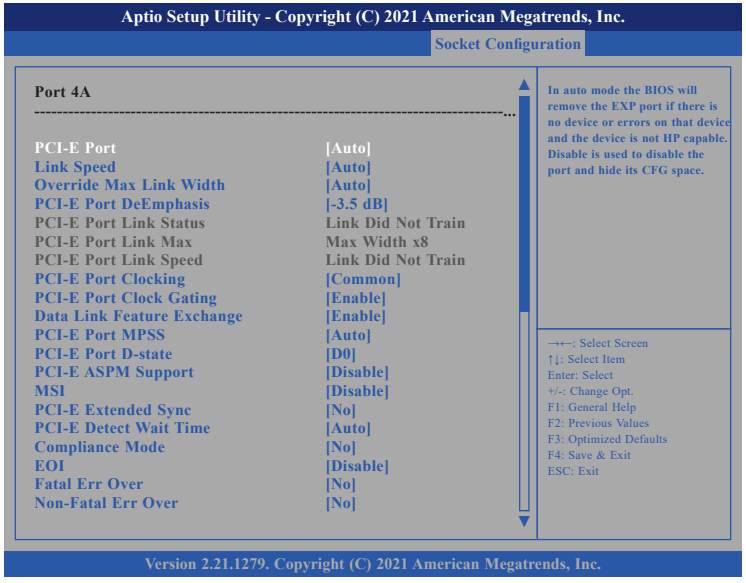
SERRE
Enables or disables SERRE bit.

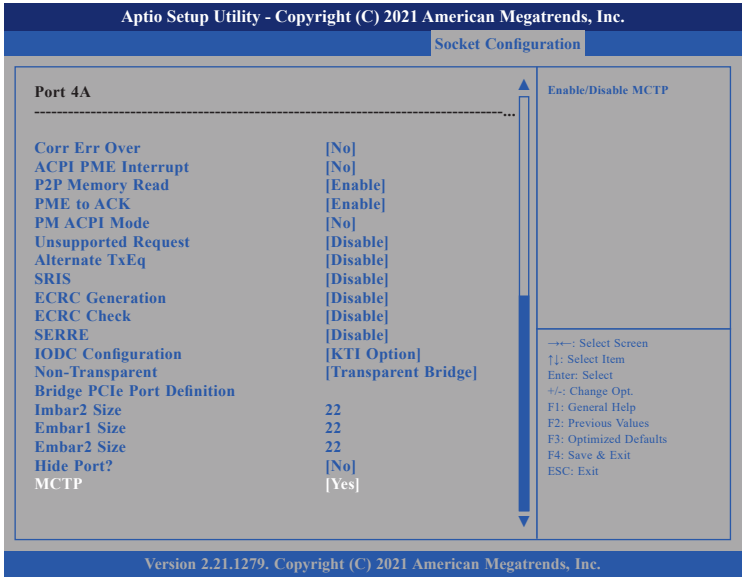
IODC Configuration
Configures the option for IODC (IO Direct Cache).

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Port 4A





PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

SERRE
Enables or disables SERRE bit.

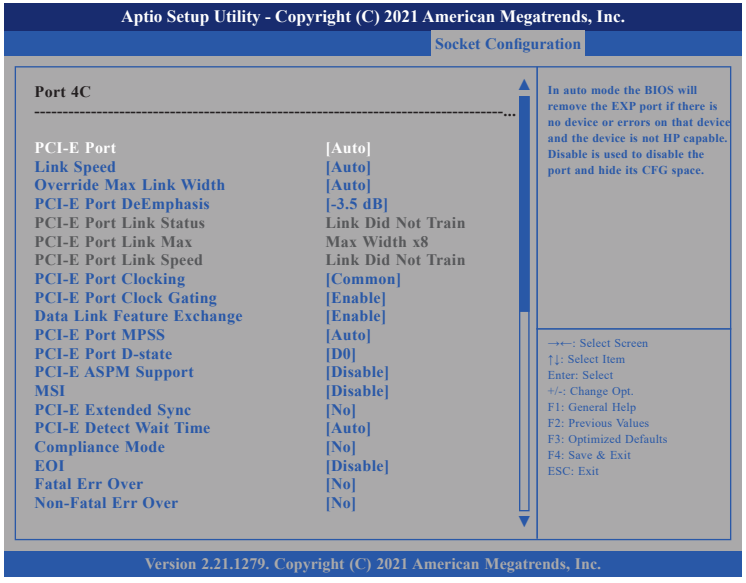
IODC Configuration
Configures the option for IODC (IO Direct Cache).

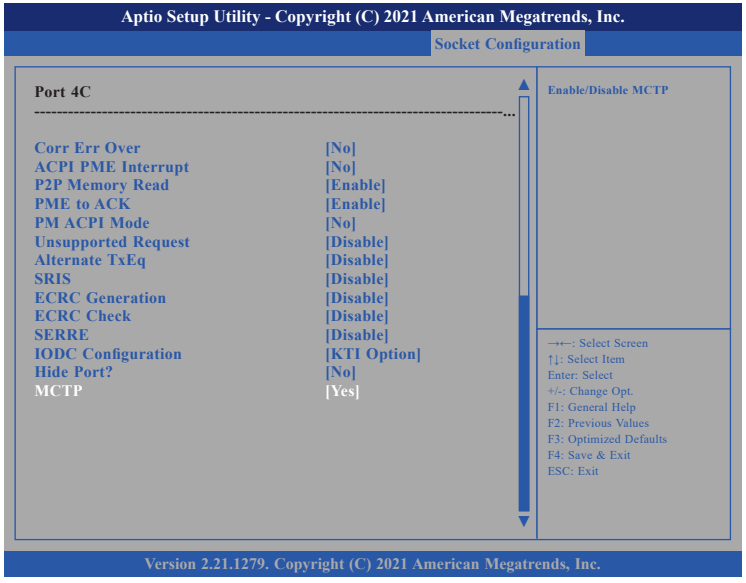
Non-Transparent Bridge PCIe Port Definition
Configures the option for the PCIe port.

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Port 4C





PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

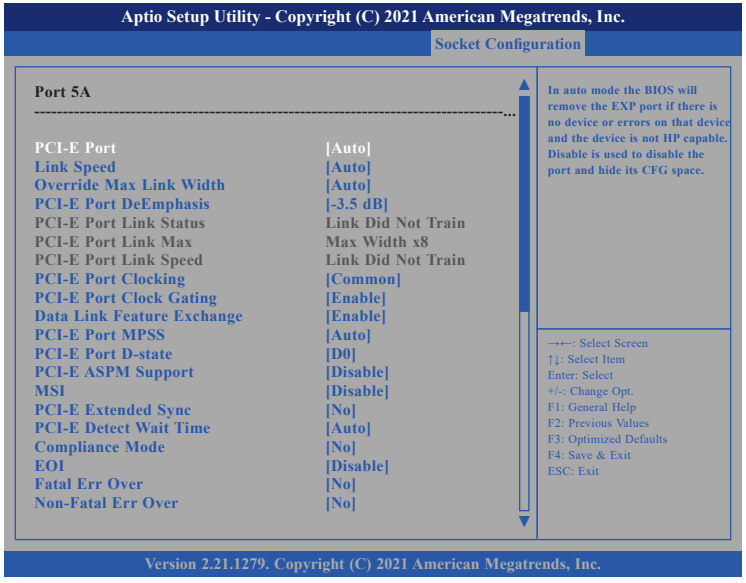
SERRE
Enables or disables SERRE bit.

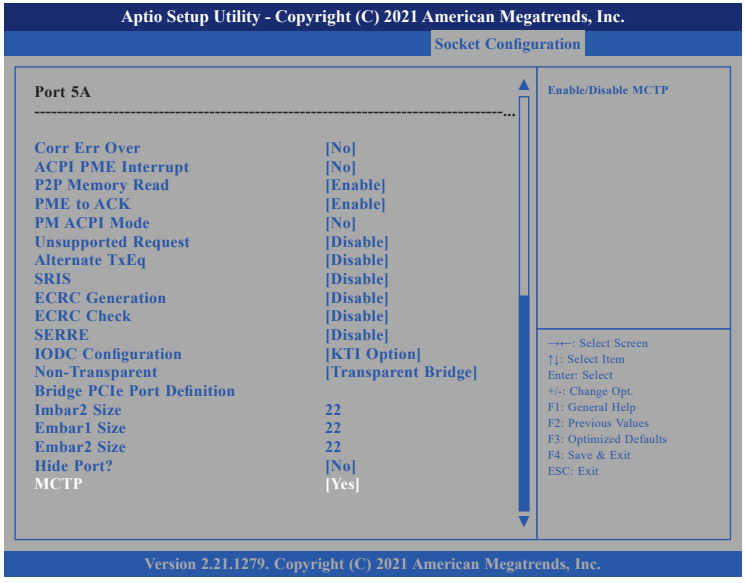
IODC Configuration
Configures the option for IODC (IO Direct Cache).

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Port 5A





PCI-E Port
Enables or disables the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Link Speed
Configures the link speed for the PCIe port.

Override Max Link Width
Configures the link speed to override the max link width set by bifurcation.

PCI-E Port DeEmphasis
Configures the de-emphasis control for the PCIe port.

PCI-E Port Clocking
Configures the option for PCI-E Port Clocking.

PCI-E Port Clock Gating
Enables or disables PCIe clock gating for each root port.

Data Link Feature Exchange
Enables or disables Data Link Feature Exchange in PCIe 4.0.

PCI-E Port MPSS
Configures the option for max payload size supported for PCI-E port.

PCI-E Port D-state
Configures the PCIe port to normal power state or low power state.

PCI-E ASPM Support
This option enables or disables ASPM support for all downstream devices.

PCI-E Extended Sync
Enables or disables the PCI-E Extended Sync mode.

PCI-E Detect Wait Time
Configures the option for PCI-E Detect Wait Time.

Compliance Mode
Enables or disables the Compliance Mode.

EOI
Enables or disables EOI.

Fatal Err Over
Enables or disables forced fatal error.

Non-Fatal Err Over
Enables or disables forced non-fatal error.

Corr Err Over
Enables forced correctable error.

ACPI PME Interrupt
Enables or disables ACPI PME Interrupts.

P2P Memory Read
Enables or disables P2P Memory Read.

PME to ACK
Enables or disables PME to ACK messages.

PM ACPI Mode
Enables or disables PM ACPI Mode.

Unsupported Request
Enables or disables unsupported request reporting.

Alternate TxEq
Enables or disables Alternate TxEq.

SRIS
Enables or disables SRIS.

ECRC Generation
Enables or disables ECRC Generation.

ECRC Check
Enables or disables ECRC Checking.

SERRE
Enables or disables SERRE bit.

IODC Configuration
Configures the option for IODC (IO Direct Cache).

Non-Transparent Bridge PCIe Port Definition
Configures the option for the PCIe port.

Hide Port?
Enables or disables the option to hide the root port.

MCTP
Enables or disables MCTP

Intel. VT for Directed I/O (VT-d)

Intel. VT for Directed I/O
Enables or disables Intel® Virtualization Technology for Directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI tables.

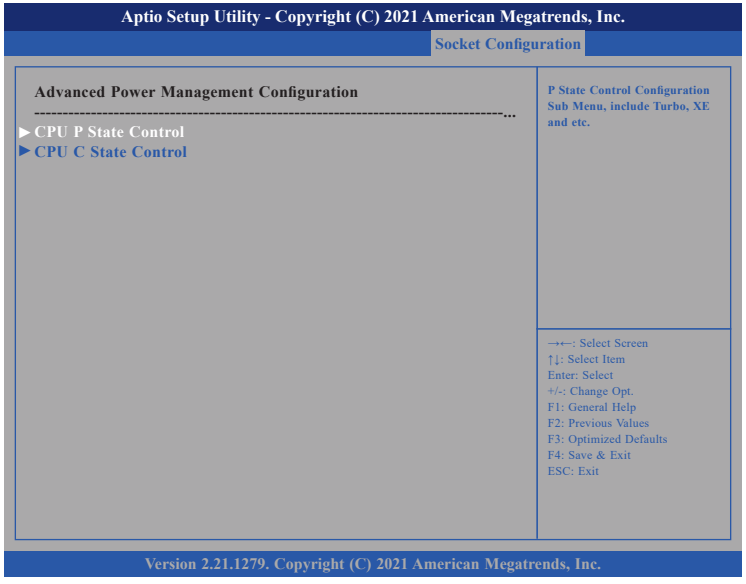
DMA Control Opt-In Flag
Enables or disables DMA Control Opt-In Flag.

Interrupt Remapping
Enables or disables Interrupt Remapping.

X2APIC Opt Out
Enables or disables X2APIC mode.

Pre-boot DMA Protection
Enables or disables Pre-boot DMA Protection.

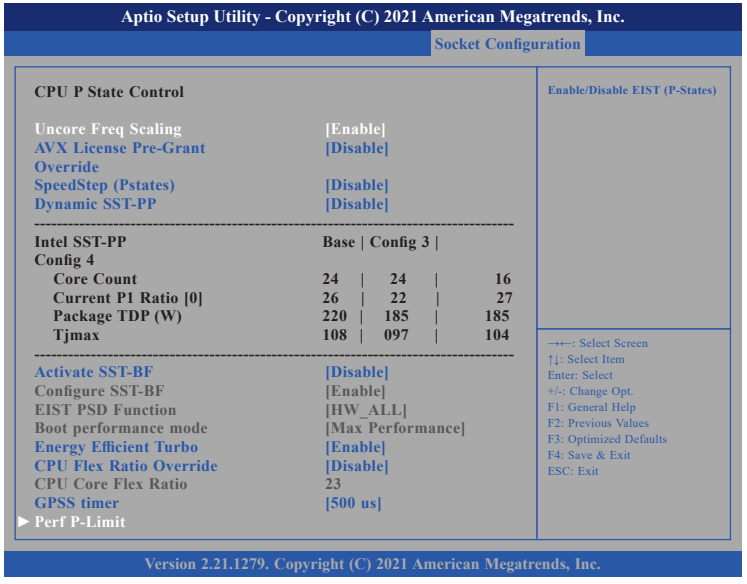
Advanced Power Management Configuration



CPU P State Control
Enters the CPU P State Control submenu.

CPU C State Control
Enters the CPU C State Control submenu.

CPU P State Control



Uncore Freq Scaling
Enables or disables autonomous uncore frequency scaling.

AVX License Pre-Grant
Enables or disables Intel® AVX License Pre-Grant Override.

SpeedStep (Pstates)
Enables or disables Intel® SpeedStep technology.

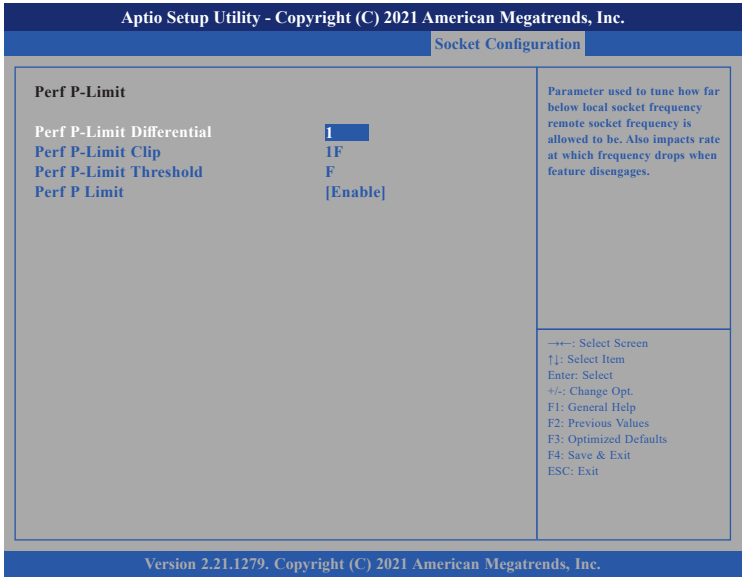
Dynamic SST-PP
Enables or disables Dynamic SST-PP.

Activate SST-BF
Enables or disables Activate SST-BF.

Energy Efficient Turbo
Enables or disables Energy Efficient Turbo.

CPU Flex Ratio Override
Enables or disables CPU Flex Ratio Override.

GPSS Timer
Configures the GPSS Timer value.



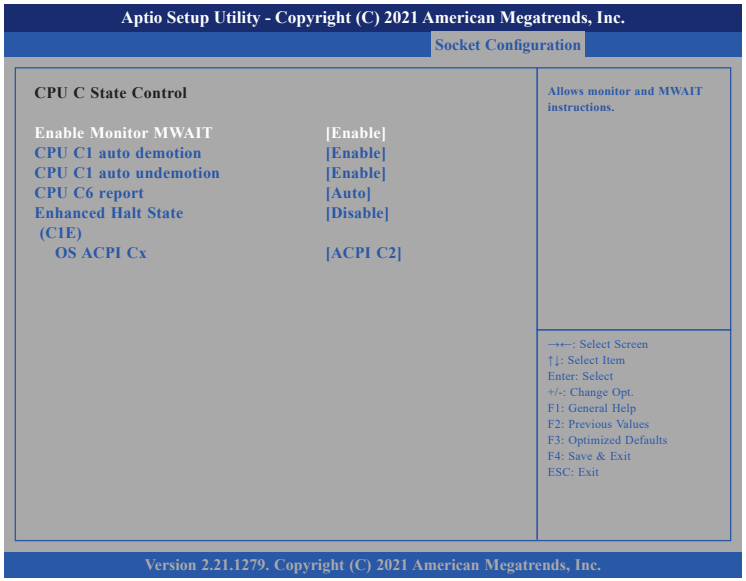
Perf P-Limit Differential
Parameter used to tune how far below local socket frequency remote socket frequency is allowed to be. Also impacts the rate at which the frequency drops when feature disengages.

Perf P-Limit Clip
Configures the performance P-Limit Clip value.

Perf P-Limit Threshold
Configures the performance P-Limit Threshold value.

Perf P Limit
Enables or disables performance P Limit.

Advanced Power Management Configuration



Enable Monitor MWAIT
Enables or disables monitoring and MWAIT instructions.

CPU C1 auto demotion
Enables or disables CPU C1 auto demotion.

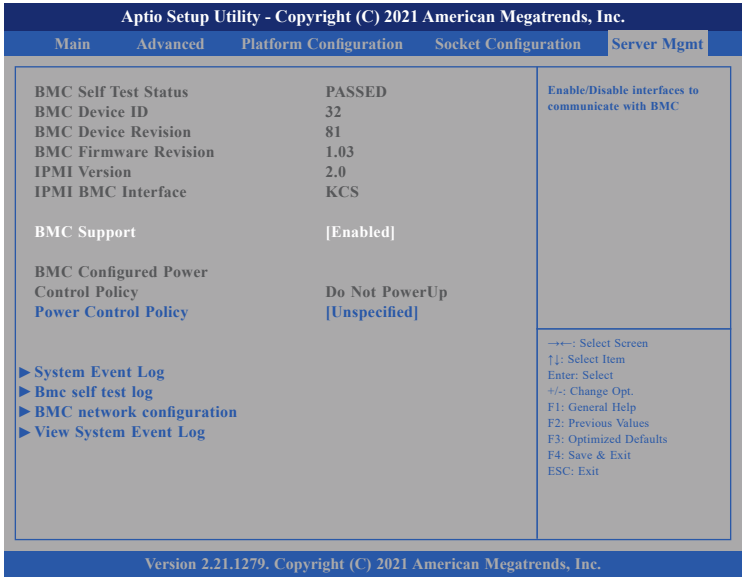
CPU C1 auto undemotion
Enables or disables CPU C1 auto undemotion.

CPU C6 report
Enables or disables C6 report to the operating system.

Enhanced Halt State (C1E)
Enables or disables Enhanced Halt State (C1E) for lower power consumption.

OS ACPI Cx
Enables or disables C3 report or C6 report to OS ACPI C2 or ACPI C3.

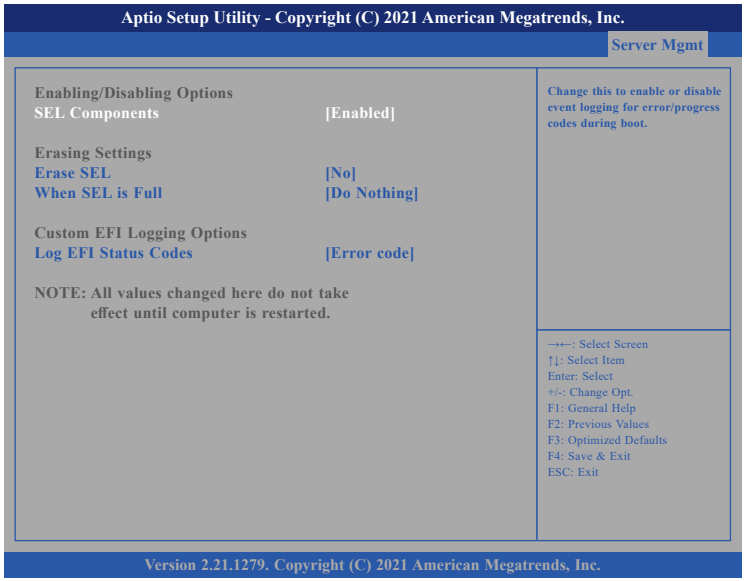
Server Mgmt



BMC Support
Enables or disables interfaces to communicate with BMC.

Power Control Policy
Configures the options for power control policy.

System Event Log



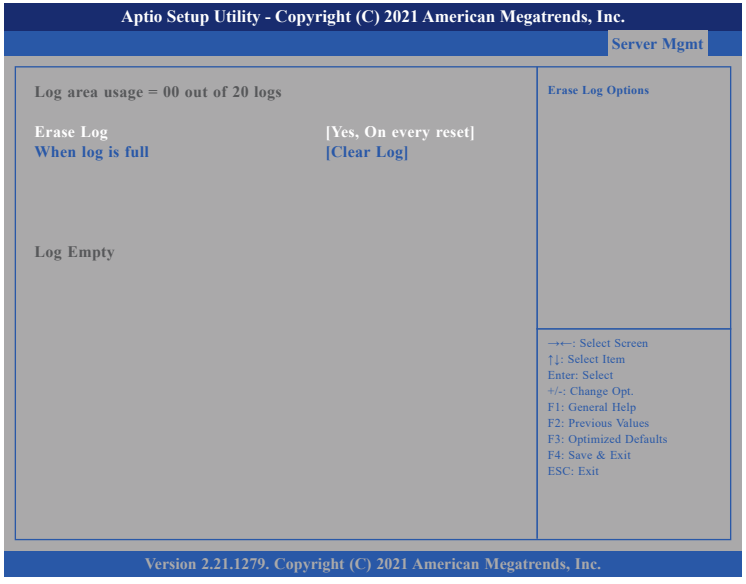
SEL Components
Enables or disables event logging for error/progress codes during boot.

Erase SEL
Configures the options for erasing SEL.

When SEL is Full
Configures the action to perform when SEL is full.

Log EFI Status Codes
Configures the options for logging EFI status codes.

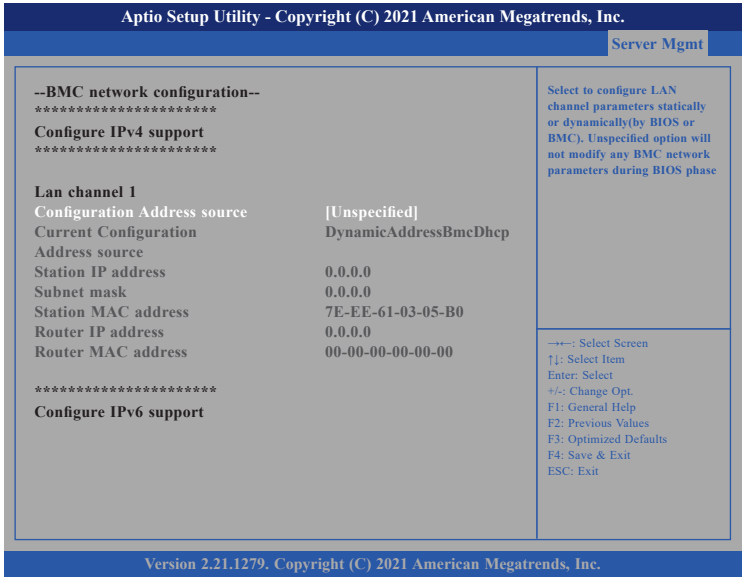
Bmc self test log



Erase Log
Configures the options for erasing log.

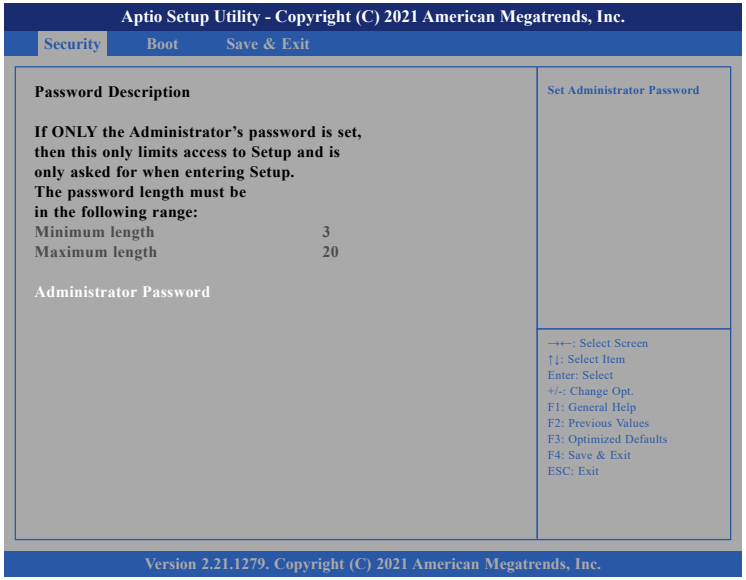
When log is full
Configures the action to perform when log is full.

BMC network configuration



Configuration Address source
Select to configure LAN channel parameters statically or dynamically (by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.

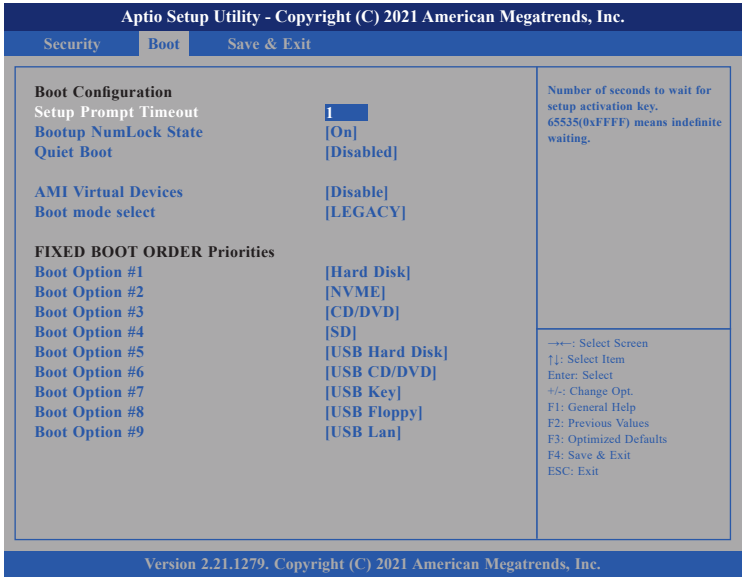
Security



Administrator Password

Select this to reconfigure the administrator's password.

Boot



Setup Prompt Timeout

Configures the number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.

Bootup NumLock State

This allows you to determine the default state of the numeric keypad. By default, the system boots up with NumLock on wherein the function of the numeric keypad is the number keys. When set to Off, the function of the numeric keypad is the arrow keys.

Quiet Boot

Enabled	Displays OEM logo instead of the POST messages.
Disabled	Displays normal POST messages.

AMI Virtual Devices
Enables or disables AMI virtual devices.

Boot mode select
Configures the boot mode option.

FIXED BOOT ORDER Priorities
Adjust the boot sequence of the system. Boot Option #1 is the first boot device that the system will boot from, next will be #2 and so forth.

Save & Exit

Save Changes and Reset
To save the changes and reset, select this field then press <Enter>. A dialog box will appear. Confirm by selecting Yes.

Discard Changes and Reset
To exit the Setup utility and reset without saving the changes, select this field then press <Enter>. You may be prompted to confirm again before exiting.

Restore Defaults
To restore the BIOS to default settings, select this field then press <Enter>. A dialog box will appear. Confirm by selecting Yes.

Launch EFI Shell from Filesystem Device
To launch EFI shell from a filesystem device, select this field and press <Enter>.

Appendix A: Memory Population Rule

Please refer to the below table for memory population rule and memory Power On Record (POR) from Intel for Ice Lake-SP. NSA 7150 supports 10+0 DDR4 memory capacity without performance compromise in the POR.

ICX iMC#		iMC2				iMC3					iMC1				iMC0									
	Channel	Chan 1 (F)		Chan 0 (E)		Chan 1 (H)		Chan 0 (G)			Chan 0 (C)		Chan 1 (D)		Chan 0 (A)		Chan 1 (B)							
DDR4 +BPS	Mode	Slot 0	Slot 1	Slot 0	Slot 1	Slot 0	Slot 1	Slot 0	Slot 1		Slot 1	Slot 0	Slot 1	Slot 0	Slot 1	Slot 0	Slot 1	Slot 0	SNC2	SNC4	Hemi	Mirror	SGX (Note #1)	POR / Validated
1+0	1LM									CPU		DDR4												POR & Val
														DDR4										POR & Val
															DDR4									POR & Val
																		DDR4						POR & Val
								DDR4																POR & Val
						DDR4																		POR & Val
				DDR4																				POR & Val
		DDR4																						POR & Val
2+0				DDR4								DDR4							Y		Y			POR & Val
								DDR4											Y		Y			POR & Val
												DDR4							Y		Y			POR & Val
				DDR4				DDR4											Y		Y			POR & Val
													DDR4		DDR4				Y		Y			POR & Val
		DDR4																DDR4	Y		Y			POR
						DDR4							DDR4						Y		Y			POR
													DDR4					DDR4	Y		Y			POR
		DDR4				DDR4													Y		Y			POR
4+0				DDR4				DDR4				DDR4				DDR4			Y	Y	Y			POR & Val
				DDR4									DDR4		DDR4				Y		Y			POR & Val
		DDR4				DDR4							DDR4					DDR4	Y	Y	Y			POR
		DDR4						DDR4				DDR4						DDR4	Y	Y	Y			POR
6+0		DDR4		DDR4				DDR4				DDR4				DDR4			Y					POR & Val
				DDR4		DDR4		DDR4				DDR4		DDR4		DDR4			Y					POR & Val
		DDR4		DDR4		DDR4								DDR4		DDR4		DDR4	Y					POR
		DDR4				DDR4		DDR4				DDR4		DDR4				DDR4	Y					POR
8+0		DDR4		DDR4		DDR4		DDR4				DDR4		DDR4		DDR4		DDR4	Y	Y	Y	Y	Y	POR & Val
12+0		DDR4	DDR4	DDR4	DDR4			DDR4	DDR4		DDR4	DDR4			DDR4	DDR4	DDR4	DDR4	Y					POR & Val
				DDR4	DDR4	DDR4	DDR4	DDR4	DDR4		DDR4	DDR4	DDR4	DDR4	DDR4	DDR4			Y					POR & Val
		DDR4	DDR4	DDR4	DDR4	DDR4	DDR4						DDR4	DDR4	DDR4	DDR4	DDR4	DDR4	Y					POR
		DDR4	DDR4			DDR4	DDR4	DDR4	DDR4		DDR4	DDR4				DDR4	DDR4	DDR4	Y					POR
		DDR4		DDR4	DDR4	DDR4	DDR4	DDR4				DDR4	DDR4	DDR4	DDR4	DDR4		DDR4	Y	Y	Y		Y	POR & Val
		DDR4		DDR4	DDR4	DDR4	DDR4	DDR4				DDR4	DDR4	DDR4	DDR4	DDR4		DDR4	Y	Y	Y		Y	POR
		DDR4	DDR4	DDR4		DDR4	DDR4	DDR4				DDR4	DDR4	DDR4		DDR4	DDR4	DDR4	Y	Y	Y		Y	POR
		DDR4	DDR4	DDR4		DDR4		DDR4	DDR4		DDR4	DDR4		DDR4		DDR4	DDR4	DDR4	Y	Y	Y		Y	POR
16+0		DDR4	DDR4	DDR4	DDR4	DDR4	DDR4	DDR4	DDR4		DDR4	DDR4	DDR4	DDR4	DDR4	DDR4	DDR4	DDR4	Y	Y	Y	Y	Y	POR & Val