NEXCOM International Co., Ltd.

Network and Communication Solutions

Fixed Wireless Access Telecom Appliance

FTA 1170 Series

User Manual

NEXCOM International Co., Ltd.
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PREFACE

Copyright

Disclaimer

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Acknowledgements

FTA 1170 is a trademark of NEXCOM International Co., Ltd. All other product names mentioned herein are registered trademarks of their respective owners.

Regulatory Compliance Statements

This section provides the FCC compliance statement for Class B devices and describes how to keep the system CE compliant.

Declaration of Conformity

FCC

This equipment has been tested and verified to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area (domestic environment) is likely to cause harmful interference, in which case the user will be required to correct the interference (take adequate measures) at their own expense.

CE

The product(s) described in this manual complies with all applicable European Union (CE) directives if it has a CE marking. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cable and cabling techniques.

RoHS Compliance

NEXCOM RoHS Environmental Policy and Status Update

NEXCOM is a global citizen for building the digital infrastructure. We are committed to providing green products and services, which are compliant with European Union RoHS (Restriction on Use of Hazardous Substance in Electronic Equipment) directive 2011/65/EU, to be your trusted green partner and to protect our environment.

RoHS restricts the use of Lead (Pb) < 0.1% or 1,000ppm, Mercury (Hg) < 0.1% or 1,000ppm, Cadmium (Cd) < 0.01% or 100ppm, Hexavalent Chromium (Cr6+) < 0.1% or 1,000ppm, Polybrominated biphenyls (PBB) < 0.1% or 1,000ppm, and Polybrominated diphenyl Ethers (PBDE) < 0.1% or 1,000ppm.

In order to meet the RoHS compliant directives, NEXCOM has established an engineering and manufacturing task force in to implement the introduction of green products. The task force will ensure that we follow the standard NEXCOM development procedure and that all the new RoHS components and new manufacturing processes maintain the highest industry quality levels for which NEXCOM are renowned.

The model selection criteria will be based on market demand. Vendors and suppliers will ensure that all designed components will be RoHS compliant.

How to recognize NEXCOM RoHS Products?

For existing products where there are non-RoHS and RoHS versions, the suffix "(LF)" will be added to the compliant product name.

All new product models launched after January 2013 will be RoHS compliant. They will use the usual NEXCOM naming convention.

Warranty and RMA

NEXCOM Warranty Period

NEXCOM manufactures products that are new or equivalent to new in accordance with industry standard. NEXCOM warrants that products will be free from defect in material and workmanship for 2 years, beginning on the date of invoice by NEXCOM.

NEXCOM Return Merchandise Authorization (RMA)

- Customers shall enclose the "NEXCOM RMA Service Form" with the returned packages.
- Customers must collect all the information about the problems encountered and note anything abnormal or, print out any on-screen messages, and describe the problems on the "NEXCOM RMA Service Form" for the RMA number apply process.
- Customers can send back the faulty products with or without accessories (manuals, cable, etc.) and any components from the card, such as CPU and RAM. If the components were suspected as part of the problems, please note clearly which components are included. Otherwise, NEXCOM is not responsible for the devices/parts.
- Customers are responsible for the safe packaging of defective products, making sure it is durable enough to be resistant against further damage and deterioration during transportation. In case of damages occurred during transportation, the repair is treated as "Out of Warranty."
- Any products returned by NEXCOM to other locations besides the customers' site will bear an extra charge and will be billed to the customer.

Repair Service Charges for Out-of-Warranty Products

NEXCOM will charge for out-of-warranty products in two categories, one is basic diagnostic fee and another is component (product) fee.

System Level

- Component fee: NEXCOM will only charge for main components such as SMD chip, BGA chip, etc. Passive components will be repaired for free, ex: resistor, capacitor.
- Items will be replaced with NEXCOM products if the original one cannot be repaired. Ex: motherboard, power supply, etc.
- Replace with 3rd party products if needed.
- If RMA goods can not be repaired, NEXCOM will return it to the customer without any charge.

Board Level

- Component fee: NEXCOM will only charge for main components, such as SMD chip, BGA chip, etc. Passive components will be repaired for free, ex: resistors, capacitors.
- If RMA goods can not be repaired, NEXCOM will return it to the customer without any charge.

Warnings

Read and adhere to all warnings, cautions, and notices in this guide and the documentation supplied with the chassis, power supply, and accessory modules. If the instructions for the chassis and power supply are inconsistent with these instructions or the instructions for accessory modules, contact the supplier to find out how you can ensure that your computer meets safety and regulatory requirements.

Cautions

Electrostatic discharge (ESD) can damage system components. Do the described procedures only at an ESD workstation. If no such station is available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the computer chassis.

Safety Information

Before installing and using the device, note the following precautions:

- Read all instructions carefully.
- Do not place the unit on an unstable surface, cart, or stand.
- Follow all warnings and cautions in this manual.
- When replacing parts, ensure that your service technician uses parts specified by the manufacturer.
- Avoid using the system near water, in direct sunlight, or near a heating device.
- The load of the system unit does not solely rely for support from the rackmounts located on the sides. Firm support from the bottom is highly necessary in order to provide balance stability.
- The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Installation Recommendations

Ensure you have a stable, clean working environment. Dust and dirt can get into components and cause a malfunction. Use containers to keep small components separated.

Adequate lighting and proper tools can prevent you from accidentally damaging the internal components. Most of the procedures that follow require only a few simple tools, including the following:

- A Philips screwdriver
- A flat-tipped screwdriver
- A grounding strap
- An anti-static pad

Using your fingers can disconnect most of the connections. It is recommended that you do not use needle-nose pliers to disconnect connections as these can damage the soft metal or plastic parts of the connectors.

Safety Precautions

1. Read these safety instructions carefully.

2. Keep this User Manual for later reference.

3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.

4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.

5. Keep this equipment away from humidity.

6. Put this equipment on a stable surface during installation. Dropping it or letting it fall may cause damage.

7. The openings on the enclosure are for air convection to protect the equipment from overheating. DO NOT COVER THE OPENINGS.

8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.

9. Place the power cord in a way so that people will not step on it. Do not place anything on top of the power cord. Use a power cord that has been approved for use with the product and that it matches the voltage and current marked on the product's electrical range label. The voltage and current rating of the cord must be greater than the voltage and current rating marked on the product.

10. All cautions and warnings on the equipment should be noted.

11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.

12. Never pour any liquid into an opening. This may cause fire or electrical shock.

13. Never open the equipment. For safety reasons, the equipment should be opened only by skilled person.

14. If one of the following situations arises, get the equipment checked by service personnel:
    a. The power cord or plug is damaged.
    b. Liquid has penetrated into the equipment.
    c. The equipment has been exposed to moisture.
    d. The equipment does not work well, or you cannot get it to work according to the user's manual.
    e. The equipment has been dropped and damaged.
    f. The equipment has obvious signs of breakage.

15. Do not place heavy objects on the equipment.

16. The unit uses a three-wire ground cable which is equipped with a third pin to ground the unit and prevent electric shock. Do not defeat the purpose of this pin. If your outlet does not support this kind of plug, contact your electrician to replace your obsolete outlet.

17. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER. DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

    "ATTENTION: Risque d'explosion si la batterie est remplacée par un type incorrect. Mettre au rebus les batteries usagées selon les instructions."

18. This equipment is not suitable for use in locations where children are likely to be present.

    Cet équipement ne convient pas à une utilisation dans des lieux pouvant accueillir des enfants.

19. Suitable for installation in Information Technology Rooms in accordance with Article 645 of the National Electrical Code and NFPA 75.

    Peut être installé dans des salles de matériel de traitement de l'information conformément à l'article 645 du National Electrical Code et à la NFPA 75.

20. Use certified and rated Laser Class I for Optical Transceiver product.

Technical Support and Assistance

1. For the most updated information of NEXCOM products, visit NEXCOM's website at www.nexcom.com.

2. For technical issues that require contacting our technical support team or sales representative, please have the following information ready before calling:
   - Product name and serial number
   - Detailed information of the peripheral devices
   - Detailed information of the installed software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wordings of the error messages

Warning!

1. Handling the unit: carry the unit with both hands and handle it with care.

2. Maintenance: to keep the unit clean, use only approved cleaning products or clean with a dry cloth.

Conventions Used in this Manual

Warning:
Information about certain situations, which if not observed, can cause personal injury. This will prevent injury to yourself when performing a task.

Caution:
Information to avoid damaging components or losing data.

Note:
Provides additional information to complete a task easily.

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Package Contents

Before continuing, verify that the FTA 1170 series package that you received is complete. Your FTA 1170 series package should have all the items listed in the table below.

Item	Part Number	Name	Qty
1	5040210036X00	EAR SET FOR NSA5181 VER:A PANADVANCE 53.85x43x22mm SECC T=2.0mm PANTING PANTONE 295U	1
2	5044440031X00	RUBBER FOOT KANG YANG:RF20-5-4P	1
3	6023309081X00	CABLE EDI:232091081804-RS	1
4	5040150001X00	NSA7135 AL HANDLE VER:A PANADVANCE	1

Chapter 1: Product Introduction

Overview

Key Features

- Intel Atom® P5300 processor series SoC, BGA type
- 4 x 288-pin DDR4 DIMM socket
- 1 x mini-PCIe slot for Wi-Fi 6 module
- 1 x M.2 3052 Key B for 5G FR1 module
- 1 x SO-DIMM DDR4 260-pin for BMC module
- 24 x 2.5GbE RJ45 switch ports
- 4 x 10GbE RJ45 NIC ports
- 2 x 10GbE SFP+ switch ports
- 2 x 10GbE SFP+ NIC ports
- 1 x PCIe Gen3 x16 interface LAN module slot

Hardware Specifications

Main Board

- Intel Atom® processor P5300 SoC, BGA type, 8-24 cores (up to 85W), w/ Intel® QAT

Main Memory

4 x DDR4 2933 ECC RDIMM, UDIMM sockets, max. memory capacity up to 256GB for RDIMM and 128GB for UDIMM

Storage Device

- 1 x 8G eMMC 5.1 onboard
- 2 x 2.5" internal SSD/HDD
- 1 x M.2 2280 NVMe (Key M, PCIe x4)

Interface External

- Button: reset
- LED for power/HDD/LAN/5G/Wi-Fi 6/PoE status
- 1 x RJ45 console port
- 1 x RJ45 management port
- 2 x USB 3.0 port
- 1 x nano-SIM slot
- 24 x 2.5GbE switch ports with PoE+ (FTA 1170) /24 x 2.5GbE switch ports (FTA 1170A)
- 4 x 10GbE RJ45 NIC with PoE+ (FTA 1170)/ 4 x 10GbE RJ45 NIC ports (FTA 1170A)
- 2 x 10GbE SFP+ switch ports
- 2 x 10GbE SFP+ NIC ports
- 8 x SMA connectors (front: 4 x for 5G/4G LTE, 2 x for Wi-Fi 5/6 antennas; back: 2 x for Wi-Fi 5/6 antennas)
- 1 x PCIe Gen3 x16 interface LAN module slot

Interface Internal

- 1 x mini-PCIe slot for Wi-Fi 6
- 1 x M.2 3052 Key B for 5G
- 1 x SO-DIMM DDR4 260-pin for IPMI module
- 4 x SPI connectors for PoE+ modules
- 1 x TPM header

Power

- 1 x CRPS 550W 12V AC PSU + 1 x CRPS 1000W 54V PoE+ PSU (FTA 1170)
- 2 x CRPS 550W 12V AC Redundant PSU (FTA 1170A)

Dimension and Weight

- Chassis dimension (mm): 438mm x 542 mm x 44mm (W x D x H)
- Package dimension(mm): 570mm x 741 mm x 226mm (W x D x H)
- Without packing: 10.1Kg
- With packing: 12.1kg

Environment

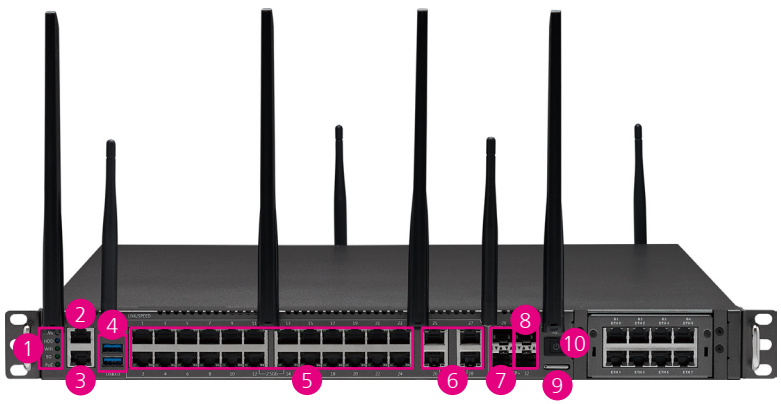
- Operating temperature: 0°C~40°C
- Storage temperature: -20°C~80°C
- Relative humidity: 10%~90% non-condensing

Certifications

- CE/FCC Class A
- CE-LVD

Knowing Your FTA1170

Front Panel



1. **LAN LED Indicators**
   Indicate the system power and link status of the system.

2. **RJ45 Console Port**
   Connect to RJ45 console devices.

3. **Management LAN Port**
   Used for managing the system.

4. **USB 3.0 Port**
   Connect to USB 3.0/2.0/1.1 devices.

5. **2.5G RJ45 PoE+**
   Connect the system to a local area network. (PoE is not supported by the FTA1170A).

6. **10GBASE-T RJ45 PoE+**
   Connect the system to a local area network. (PoE is not supported by the FTA1170A).

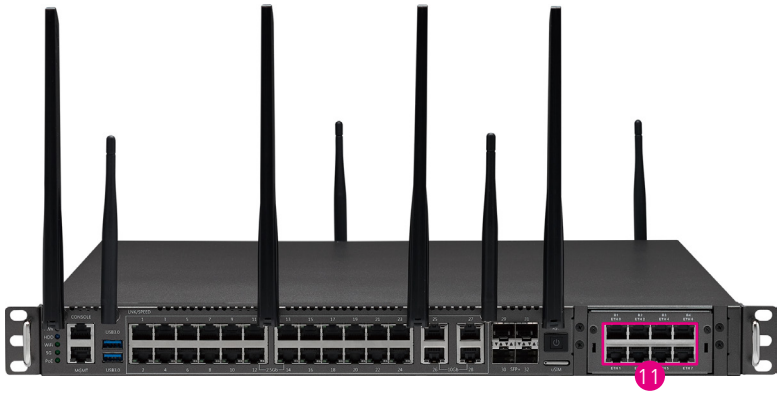
7. **10G SFP+ Switch Ports**
   Connect SFP+ modules for connecting fiber optic network devices.

8. **10G SFP+ NIC Ports**
   Connect the system to a local area network via SFP+ interface.

9. **Nano SIM slot**
   For plugging a nano SIM card.

10. **Power and Reset Button**
    Power on or turn off the system, or press and hold this button for 4 seconds to restart the system.

Rear Panel



11 LAN Module Slot
LAN module bay to install add-on network modules.

12 AC Power Inlets
Connect the system to an AC power source.

Chapter 2: Jumpers and Connectors

This chapter describes how to set the jumpers and connectors on the FTA1170 motherboard.

Before You Begin

- Ensure you have a stable, clean working environment. Dust and dirt can get into components and cause a malfunction. Use containers to keep small components separated.
- Adequate lighting and proper tools can prevent you from accidentally damaging the internal components. Most of the procedures that follow require only a few simple tools, including the following:
  - A Philips screwdriver
  - A flat-tipped screwdriver
  - A set of jewelers screwdrivers
  - A grounding strap
  - An anti-static pad
- Using your fingers can disconnect most of the connections. It is recommended that you do not use needle-nosed pliers to disconnect connections as these can damage the soft metal or plastic parts of the connectors.
- Before working on internal components, make sure that the power is off. Ground yourself before touching any internal components, by touching a metal object. Static electricity can damage many of the electronic components. Humid environments tend to have less static electricity than dry environments. A grounding strap is warranted whenever danger of static electricity exists.

Precautions

Computer components and electronic circuit boards can be damaged by discharges of static electricity. Working on computers that are still connected to a power supply can be extremely dangerous.

Follow the guidelines below to avoid damage to your computer or yourself:

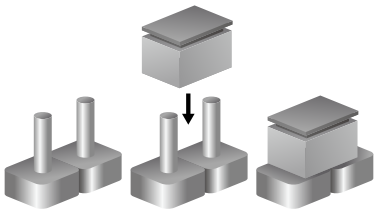
- Always disconnect the unit from the power outlet whenever you are working inside the case.
- If possible, wear a grounded wrist strap when you are working inside the computer case. Alternatively, discharge any static electricity by touching the bare metal chassis of the unit case, or the bare metal body of any other grounded appliance.
- Hold electronic circuit boards by the edges only. Do not touch the components on the board unless it is necessary to do so. Don't flex or stress the circuit board.
- Leave all components inside the static-proof packaging that they shipped with until they are ready for installation.
- Use correct screws and do not over tighten screws.

Jumper Settings

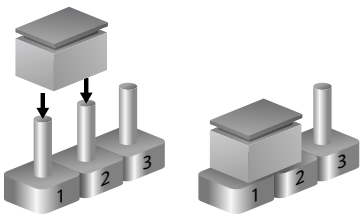
A jumper is the simplest kind of electric switch. It consists of two metal pins and a cap. When setting the jumpers, ensure that the jumper caps are placed on the correct pins. When the jumper cap is placed on both pins, the jumper is short. If you remove the jumper cap, or place the jumper cap on just one pin, the jumper is open.

Refer to the illustrations below for examples of what the 2-pin and 3-pin jumpers look like when they are short (on) and open (off).

Two-Pin Jumpers: Open (Left) and Short (Right)



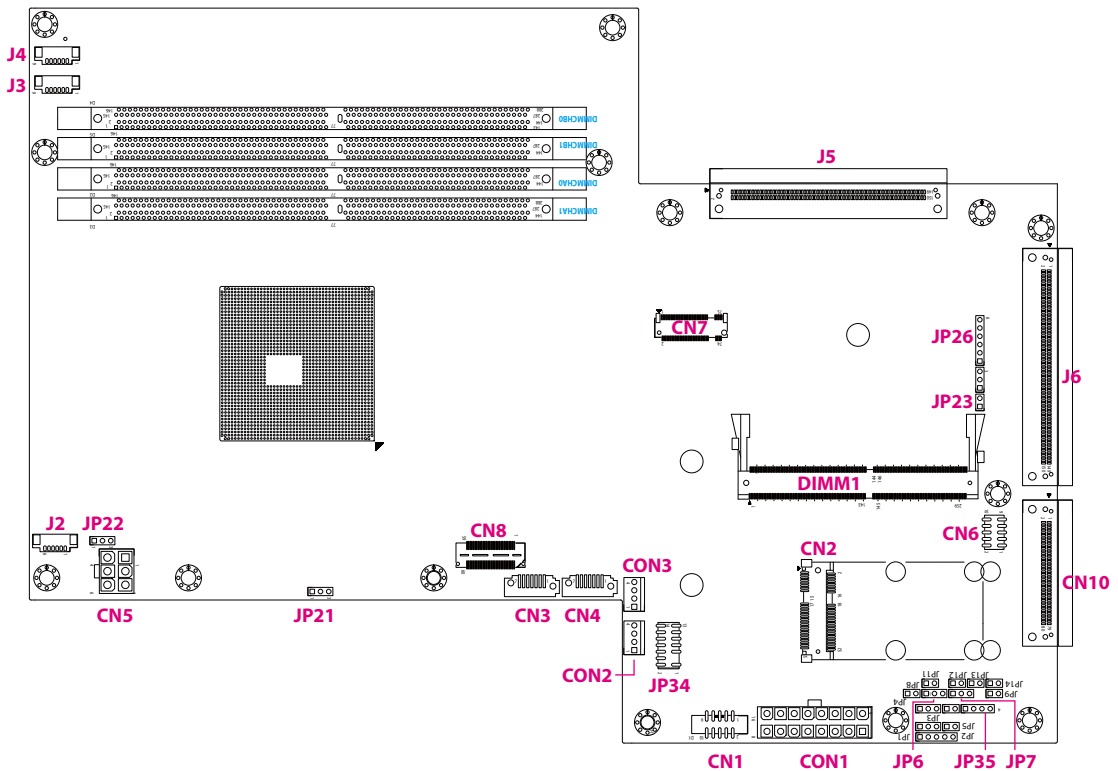
Three-Pin Jumpers: Pins 1 and 2 are Short



Locations of the Mainbaord Jumpers and Connectors

The following figure shows the mainboard used in the FTA 1170, and indicates the locations of the jumpers and connectors. Refer to this section for detailed pin settings and definitions of the connectors marked in pink on the figure below.

FTA 1170 Main Board Top View



Jumpers

SYS RTC Header Clear

Connector type: 1 x 3 = 3 pin, 2.54mm
Connector location: JP6

1  3

Pin	Function
1-2	Normal (Default)
2-3	Clear CMOS

Pin	Definition
1	N.C.
2	RST_SOC_RTEST_N
3	GND

CMOS Header

Connector type: 1 x 3 = 3 pin, 2.54mm
Connector location: JP7

1  3

Pin	Function
1-2	Normal (Default)
2-3	Clear CMOS

Pin	Definition
1	N.C.
2	RST_SRTCRST_N
3	GND

JTAG SEL Header

Connector type: 1 x 2 = 2 pin, 2.54mm
Connector location: JP23

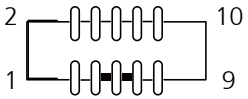
Pin	Function
Open	Normal (Default)
1-2	Update MB CPLD firmware online.

Pin	Definition
1	JTAG_SEL
2	GND

Connector Pin Definitions

PSU Power Control Connector

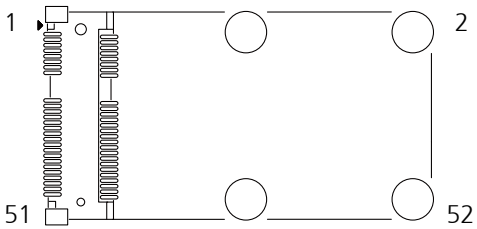
Connector type: 2 x 5 = 10 pin, 2.0mm
Connector location: CN1



Pin	Definition	Pin	Definition
1	SMB_PMBUS_SML1_ STBY_LVC3_SDA	2	SMB-ALERT_A_CAB
3	SMB_PMBUS_SML1_ STBY_LVC3_SCL	4	SMB-ALERT_B_CAB
5	PSON_CAB	6	PRESENT_IN_A_CAB
7	PW_OK_A_CAB	8	PRESENT_IN_B_CAB
9	PW_OK_B_CAB	10	N.C.

Mini PCIe Slot

Connector location: CN2

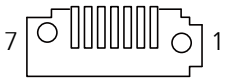


Pin	Definition	Pin	Definition
1	MPCIE_WAKE# (N.C.)	2	P3V3
3	MINI_COEX1	4	GND
5	MINI_COEX2	6	P1V5
7	WIFI_CLKREQ#	8	N.C.
9	GND	10	N.C.
11	CLK_M2_WIFI2_N	12	N.C.
13	CLK_M2_WIFI2_P	14	N.C.
15	GND	16	N.C.
17	N.C.	18	GND
19	N.C.	20	MPCIE_DIS#
21	GND	22	MPCIE_RST
23	WIFI_RXN_1	24	P3V3
25	WIFI_RXP_1	26	GND

Pin	Definition	Pin	Definition
27	GND	28	P1V5
29	GND	30	MINI_PCIE_CLK
31	WIFI_TXN_1_C	32	MINI_PCIE_DAT
33	WIFI_TXP_1_C	34	GND
35	GND	36	USB2_P2_DN
37	GND	38	USB2_P2_DP
39	P3V3	40	GND
41	P3V3	42	WIFI_LED_WWAN#
43	GND	44	WIFI_LED_WLAN#
45	N.C.	46	WIFI_LED_WPAN#
47	N.C.	48	P1V5
49	N.C.	50	GND
51	N.C.	52	P3V3

SATA Connector

Connector type: 1 x 7 = 7 pin
Connector location: CN3, CN4



CN3

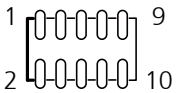
Pin	Definition
1	GND
2	SATA1_TX_DP_C
3	SATA1_TX_DN_C
4	GND
5	SATA1_RX_DN_C
6	SATA1_RX_DP_C
7	GND

CN4

Pin	Definition
1	GND
2	SATA0_TX_DP_C
3	SATA0_TX_DN_C
4	GND
5	SATA0_RX_DN_C
6	SATA0_RX_DP_C
7	GND

CPLD GPIO Header

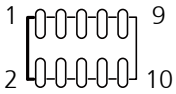
Connector type: 2 x 3 = 6 pin, 4.2mm
Connector location: CN5



Pin	Definition
1	P12V1
2	P12V1
3	P12V1
4	GND
5	GND
6	GND

CPLD GPIO Header

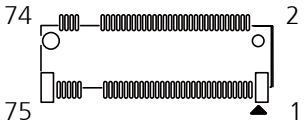
Connector type: 2 x 5 = 10 pin, 2.0mm (4 GPI; 4 GPO)
Connector location: CN6



Pin	Definition	Pin	Definition
1	P3V3_AUX	2	GND
3	CPLD_GPIN1	4	CPLD_GPOUT1
5	CPLD_GPIN2	6	CPLD_GPOUT2
7	CPLD_GPIN3	8	CPLD_GPOUT3
9	CPLD_GPIN4	10	CPLD_GPOUT4

M.2 2280 Key M PCIe Slot

Connector type: 75 pin
Connector location: CN7



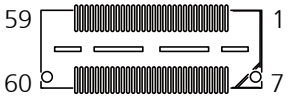
Pin	Definition	Pin	Definition
1	GND	13	SSD_TXP_3_C
2	P3V3_SSD	14	P3V3_SSD
3	GND	15	GND
4	P3V3_SSD	16	P3V3_SSD
5	SSD_RXN_3	17	SSD_RXN_2
6	N.C.	18	P3V3_SSD
7	SSD_RXP_3	19	SSD_RXP_2
8	N.C.	20	N.C.
9	GND	21	SSD_CONFIG_0
10	M.2_ACT_LED1	22	N.C.
11	SSD_TXN_3_C	23	SSD_TXN_2_C
12	P3V3_SSD	24	N.C.

Pin	Definition	Pin	Definition
25	SSD_TXP_2_C	36	N.C.
26	N.C.	37	SSD_TXP_1_C
27	GND	38	NGFF_DEVSLP
28	N.C.	39	GND
29	SSD_RXN_1	40	N.C.
30	N.C.	41	SSD_RXP_0
31	SSD_RXP_1	42	N.C.
32	N.C.	43	SSD_RXN_0
33	GND	44	N.C.
34	N.C.	45	GND
35	SSD_TXN_1_C	46	N.C.

Pin	Definition	Pin	Definition
47	SSD_TXN_0_C	58	N.C.
48	N.C.	67	N.C.
49	SSD_TXP_0_C	68	CLK_32K_SUSCLK_SOC
50	SSD_RST_N	69	N.C.
51	GND	70	P3V3_SSD
52	SSD_CLKREQ#	71	GND
53	CLK_M2_SSD_N	72	P3V3_SSD
54	MFG_CLK2	73	GND
55	CLK_M2_SSD_P	74	P3V3_SSD
56	N.C.	75	GND
57	GND		

Intel XDP Connector (for Debug)

Connector size: BD TO BD 2x 30 = 60 pin 0.5mm
Connector location: CN8

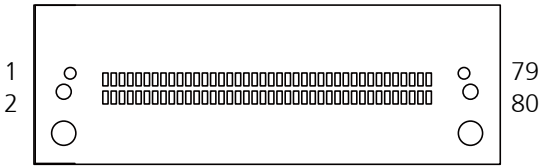


Pin	Definition	Pin	Definition
1	P1V05_A	2	JTAG_SOC_TMS
3	JTAG_CPU_TCK	4	JTAG_SOC_TDO
5	JTAG_SOC_TDI	6	RST_LTB_RSTBTN_R_N
7	RST_LTB_PLTRST_R_N	8	PD_JTAG_LTB_TRST
9	JTAG_SOC_TRST_N	10	DBP_DBG_LTB_SOC_PREQ_N
11	DBP_LTB_SOC_PRDY_N	12	P1V05_A
13	TRC_DFX_CLK0_R	14	GND
15	DBP_LTB_PCH_DEBUG_CONSENT_R_N	16	GND
17	FM_LTB_CPU_DEBUG_EN_N	18	N.C.
19	TRC_PTI_DATA_R0	20	N.C.
21	TRC_PTI_DATA_R1	22	N.C.
23	TRC_PTI_DATA_R2	24	N.C.
25	TRC_PTI_DATA_R3	26	N.C.
27	TRC_PTI_DATA_R4	28	N.C.
29	TRC_PTI_DATA_R5	30	N.C.

Pin	Definition	Pin	Definition
31	TRC_PTI_DATA_R6	32	N.C.
33	TRC_PTI_DATA_R7	34	TP_LTB_PIN34
35	TRC_PTI_DATA_R8	36	FM_BOOT_HALT_TIMESYNC2_R
37	TRC_PTI_DATA_R9	38	DBP_LTB_SOC_FBRK_N
39	TRC_PTI_DATA_R10	40	FM_LTB_PWRBTN_R_N
41	TRC_PTI_DATA_R11	42	RST_CPLD_LTB_RSMRST_R_N
43	TRC_PTI_DATA_R12	44	CLK_100M_MIPI60_DN_R
45	TRC_PTI_DATA_R13	46	CLK_100M_MIPI60_DP_R
47	TRC_PTI_DATA_R14	48	SMB_SMT0_LTB_CLK
49	TRC_PTI_DATA_R15	50	SMB_SMT0_LTB_DATA
51	JTAG_PCH_TCK	52	PU_P52_3V3
53	DBP_LTB_MBP1_R_N (N.C.)	54	TP_J5K1_54
55	DBP_LTB_MBP0_R_N (N.C.)	56	TP_J5K1_56
57	GND	58	GND
59	TRC_DFX_CLK1_R	60	PD_LTB_P60

Board to Board Connector (Low Speed)

Connector size: 80 Pin, 0.8mm
Connector location: CN10



Pin	Definition	Pin	Definition
1	BMC_CPLD_RI_N	11	BMC_CPLD_DTR_N
2	FM_SOC_CPLD_SLP_S3_N	12	GND
3	BMC_CPLD_RXD	13	BMC_CPLD_TXD
4	N.C.	14	USB2_P0_DN
5	BMC_CPLD_DSR_N	15	BMC_CPLD_RTS_N
6	N.C.	16	USB2_P0_DP
7	BMC_CPLD_CTS_N	17	PU_NIC0_NCSI_RXD_1
8	IRQ_5GM2_WAKE_N	18	GND
9	BMC_CPLD_DCD_N	19	PD_NIC0_NCSI_CRS_DV
10	POWER_OK_EN	20	USB2_P1_DN

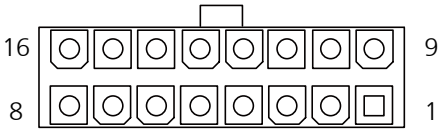
Pin	Definition	Pin	Definition
21	NCSI_CLK_I210	31	FM_NIC0_DISABLE_N
22	USB2_P1_DP	32	USB3_TX_N0_C
23	PU_NIC0_NCSI_RXD_0	33	IRQ_NIC0_WAKE_N
24	GND	34	USB3_TX_P0_C
25	PU_NIC0_NCSI_TXD_0	35	RST_CPLD_NIC_RESET_N
26	USB3_RX_N0_C	36	GND
27	PU_NIC0_NCSI_TXD_1	37	SMB_ME_SMT1_ALRT_N
28	USB3_RX_P0_C	38	LED_GBE0_LED0_R
29	PD_NIC0_NCSI_TX_EN	39	GND
30	GND	40	LED_GBE0_LED1_R

Pin	Definition	Pin	Definition
41	SMB_ME_SMT1_CLK	51	LED_GBE1_LED2_R
42	GND	52	P1E_NIC0_RX_DP
43	SMB_ME_SMT1_DATA	53	LED_GBE2_LED0_R
44	CLK_100M_NIC0_DN	54	GND
45	LED_GBE0_LED2_R	55	LED_GBE2_LED1_R
46	CLK_100M_NIC0_DP	56	P1E_NIC0_TX_C_DN
47	LED_GBE1_LED0_R	57	LED_GBE2_LED2_R
48	GND	58	P1E_NIC0_TX_C_DP
49	LED_GBE1_LED1_R	59	LED_GBE3_LED0_R
50	P1E_NIC0_RX_DN	60	GND

Pin	Definition	Pin	Definition
61	LED_GBE3_LED1_R	71	POWER_LED
62	GND	72	P3V3_S
63	LED_GBE3_LED2_R	73	GND
64	P3V3_AUX	74	GND
65	POE_LED	75	P12V2
66	P3V3_AUX	76	P3V3_S
67	WIFI_LED	77	P12V2
68	GND	78	P3V3_S
69	HDD_CPLD_LED	79	GND
70	P3V3_S	80	GND

12V Power Connector

Connector size: 2 x 8 = 16 pin (4.2 mm ATX connector)
Connector location: CON1



Pin	Definition	Pin	Definition
1	P12V2	9	GND
2	P12V2	10	GND
3	P12V2	11	GND
4	P12V2	12	GND
5	P12V2	13	GND
6	P12V2	14	GND
7	P12V2	15	GND
8	P12V_AUX	16	GND

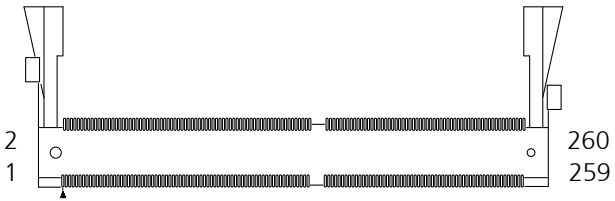
SATA Power Connector

Connector size: 1 x 4 = 4 pin, 2.54mm
Connector location: CON2, CON3

Pin	Definition
1	P12V_S2
2	GND
3	GND
4	P5V_S

Run BMC SO-DIMM Connector

Connector size: 1 x 260 = 260 Pin
Connector location: DIMM1



Pin	Definition	Pin	Definition
1	RSVD for P12V_AUX	18	N.C.
2	N.C.	19	GPIO5_SGPMCK
3	P3V3_AUX	20	N.C.
4	P3V3_AUX	21	CONSOLERX
5	P3V3_AUX	22	N.C.
6	P3V3_AUX	23	CONSOLETX
7	P3V3_AUX	24	GND
8	GND	25	N.C.
9	GND	26	PWM0_GPIO10
10	N.C.	27	PWM2_GPIO9
11	GND	28	PWM1_GPIO12
12	N.C.	29	N.C.
13	GPIO0_SGPMLD	30	N.C.
14	N.C.	31	PWM6_GPIO13
15	GPIO1_SGPMI	32	PWM5_GPIO16
16	N.C.	33	RNBMC_PRSNT#_R
17	GPIO3_SGPMO	34	N.C.

Pin	Definition	Pin	Definition
35	N.C.	52	GND
36	PW_OK_B_CAB	53	BMC_SENSOR_SCL
37	N.C.	54	I2C6SCL_GPIO28
38	GPIO20	55	BMC_SENSOR_SDA
39	GND	56	I2C6SDA_GPIO30
40	GPIO21	57	GND
41	N.C.	58	GND
42	N.C.	59	N.C.
43	N.C.	60	I2C5SCL_GPIO32
44	N.C.	61	N.C.
45	GND	62	I2C5SDA_GPIO34
46	GPIO25	63	N.C.
47	I2C8SCL_GPIO26	64	GND
48	N.C.	65	N.C.
49	I2C8SDA_GPIO27	66	GPIO36
50	I2C13SDA	67	FWSPIMISO_IO1
51	GND	68	GPIO37

Pin	Definition	Pin	Definition
69	N.C.	85	N.C.
70	GPIO38	86	N.C.
71	N.C.	87	EXTRST#
72	N.C.	88	N.C.
73	N.C.	89	GPIO55
74	N.C.	90	TACH6_GPIO56
75	N.C.	91	N.C.
76	N.C.	92	TACH7_GPIO58
77	N.C.	93	N.C.
78	TACH0_GPIO44	94	N.C.
79	N.C.	95	A_VBAT_DETECT
80	TACH1_GPIO46	96	TACH9_GPIO62
81	N.C.	97	N.C.
82	TACH2_GPIO48	98	TACH10_GPIO64
83	WDTRST2_GPIO49	99	N.C.
84	N.C.	100	TACH11_GPIO66

Pin	Definition	Pin	Definition
101	N.C.	117	N.C.
102	TACH12_GPIO68	118	N.C.
103	N.C.	119	N.C.
104	TACH13_GPIO70	120	N.C.
105	IRQ_SMB_PWR_ALERT_N	121	PW_OK_A_CAB
106	TACH14_GPIO72	122	N.C.
107	GPIO73	123	I2C2SCL_GPIO85
108	N.C.	124	N.C.
109	N.C.	125	I2C2SDA_GPIO87
110	GND	126	GND
111	P1V05_A	127	GND
112	PECI	128	I2C1SCL_GPIO88
113	N.C.	129	N.C.
114	GND	130	I2C1SDA_GPIO90
115	N.C.	131	N.C.
116	N.C.	132	GND

Pin	Definition	Pin	Definition
133	GND	149	PERXP
134	I2C4SCL_GPIO92	150	GPIO103_UART4TX
135	N.C.	151	GND
136	I2C4SDA_GPIO94	152	P3V3_AUX
137	N.C.	153	PCIE_RX_BMC_DN
138	N.C.	154	N.C.
139	GND	155	PCIE_RX_BMC_DP
140	N.C.	156	N.C.
141	I2C12SCL_GPIO98	157	GND
142	PERSTN	158	N.C.
143	I2C12SDA_GPIO99	159	PEREFCLKN
144	N.C.	160	N.C.
145	GND	161	PEREFCLKP
146	N.C.	162	N.C.
147	PERXN	163	GND
148	GPIO102_UART4RX	164	JTAG1TDO

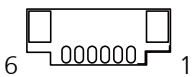
Pin	Definition	Pin	Definition
165	LPCRST#_ESPIRST#	181	BMC_RSVD1
166	JTAG1TDI	182	P3V3_ADC4
167	ESPI_IO3_LPC_AD1	183	BMC_RSVD2
168	N.C.	184	P1V05_A_ADC5
169	ESPI_IO3_LPC_AD0	185	GND
170	JTAG1TCK	186	PVCCIN_ADC6
171	LPCIRQ#_ESPIALERT#	187	I2C10SCL_GPIO110
172	JTAG1TMS	188	PVNN_NAC_ADC7
173	H_LPC_FRAME_N	189	N.C.
174	P12V2_ADC0	190	SYSCS#_GPIO112
175	ESPI_IO3_LPC_AD3	191	GND
176	P3V3_AUX_ADC1	192	SPI_PCH_IBMC_DI
177	ESPI_IO3_LPC_AD2	193	N.C.
178	P5V_AUX_ADC2	194	SPI_PCH_IBMC_DO
179	LPCCLK_ESPICLK	195	N.C.
180	P3V3_SOC_ADC3	196	SPI_PCH_IBMC_CLK

Pin	Definition	Pin	Definition
197	GND	213	N.C.
198	SPI1CS0#_GPIO116	214	N.C.
199	I2C11SCL_GPIO117	215	GND
200	SPI_IBMC_SSB_DO	216	RMIICRSDV
201	I2C11SDA_GPIO118	217	USB2_P3_DN
202	SPI_SSB_IBMC_DI	218	N.C.
203	GND	219	USB2_P3_DP
204	N.C.	220	NIC0_NCSI_CLK_IN_R
205	I2C3SCL_GPIO119	221	GND
206	N.C.	222	GND
207	I2C3SDA_GPIO121	223	N.C.
208	SPI_IBMC_SSB_CLK	224	RMIITXEN
209	N.C.	225	N.C.
210	SPI1CS1#_GPIO124	226	GND
211	N.C.	227	GND
212	GND	228	RMIIRXD0

Pin	Definition	Pin	Definition
229	N.C.	245	GND
230	RMIIRXD1	246	N.C.
231	N.C.	247	N.C.
232	GND	248	N.C.
233	GND	249	N.C.
234	PU_NIC0_NCSI_TXD_0	250	N.C.
235	N.C.	251	GND
236	PU_NIC0_NCSI_TXD_1	252	PVNN_PCH_ADC8
237	N.C.	253	BMC_RESET#
238	GND	254	P1V2_VDDQ_ADC9
239	GND	255	P3V_RTC_ADC13
240	N.C.	256	P5V_ADC10
241	N.C.	257	P1V05_NAC_ADC11
242	N.C.	258	P1V8_A_ADC12
243	N.C.	259	N.C.
244	N.C.	260	N.C.

FAN Wafer Connector

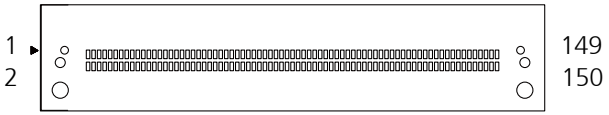
Connector size: 1 x 6 = 6 Pin, 1.25mm
Connector location: J2, J3, J4



Pin	Definition
1	GND
2	P12V_S1
3	SYS_FAN1_TACH_R
4	SYS_FAN1_PWM_R
5	GND
6	P12V_S1

PCIe Gen3 x16 Riser Card Board to Board Connector

Connector size: 2 x 75 = 150 Pin, 0.8mm
Connector location: J5



Pin	Definition	Pin	Definition
1	GND	16	PE_SOC_TX_C_DN1
2	GND	17	PE_SOC_RX_DN1
3	IRQ_PCIE_WAKE_N	18	PE_SOC_TX_C_DP1
4	SMB_PCIE_S1_CLK_R	19	GND
5	PCIE_SLOT_RST_N	20	GND
6	SMB_PCIE_S1_DATA_R	21	PE_SOC_RX_DP2
7	GND	22	PE_SOC_TX_C_DN2
8	GND	23	PE_SOC_RX_DN2
9	PE_SOC_RX_DP0	24	PE_SOC_TX_C_DP2
10	PE_SOC_TX_C_DN0	25	GND
11	PE_SOC_RX_DN0	26	GND
12	PE_SOC_TX_C_DP0	27	PE_SOC_RX_DP3
13	GND	28	PE_SOC_TX_C_DN3
14	GND	29	PE_SOC_RX_DN3
15	PE_SOC_RX_DP1	30	PE_SOC_TX_C_DP3

Pin	Definition	Pin	Definition
31	GND	46	PE_SOC_TX_C_DP6
32	GND	47	PE_SOC_RX_DN6
33	PE_SOC_RX_DP4	48	PE_SOC_TX_C_DN6
34	PE_SOC_TX_C_DN4	49	GND
35	PE_SOC_RX_DN4	50	GND
36	PE_SOC_TX_C_DP4	51	PE_SOC_RX_DP7
37	GND	52	PE_SOC_TX_C_DP7
38	GND	53	PE_SOC_RX_DN7
39	PE_SOC_RX_DP5	54	PE_SOC_TX_C_DN7
40	PE_SOC_TX_C_DP5	55	GND
41	PE_SOC_RX_DN5	56	GND
42	PE_SOC_TX_C_DN5	57	PE_SOC_RX_DP8
43	GND	58	PE_SOC_TX_C_DP8
44	GND	59	PE_SOC_RX_DN8
45	PE_SOC_RX_DP6	60	PE_SOC_TX_C_DN8

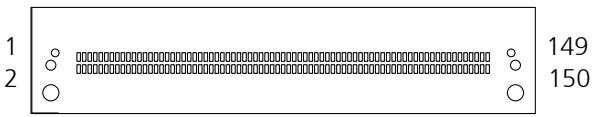
Pin	Definition	Pin	Definition
61	GND	76	PE_SOC_TX_C_DP11
62	GND	77	PE_SOC_RX_DN11
63	PE_SOC_RX_DP9	78	PE_SOC_TX_C_DN11
64	PE_SOC_TX_C_DP9	79	GND
65	PE_SOC_RX_DN9	80	GND
66	PE_SOC_TX_C_DN9	81	PE_SOC_RX_DP12
67	GND	82	PE_SOC_TX_C_DP12
68	GND	83	PE_SOC_RX_DN12
69	PE_SOC_RX_DP10	84	PE_SOC_TX_C_DN12
70	PE_SOC_TX_C_DP10	85	GND
71	PE_SOC_RX_DN10	86	GND
72	PE_SOC_TX_C_DN10	87	PE_SOC_RX_DP13
73	GND	88	PE_SOC_TX_C_DP13
74	GND	89	PE_SOC_RX_DN13
75	PE_SOC_RX_DP11	90	PE_SOC_TX_C_DN13

Pin	Definition	Pin	Definition
91	GND	106	DISCONN_A0_EN
92	GND	107	CLK_PCIE_SLOT_N
93	PE_SOC_RX_DP14	108	DISCONN_A1_EN
94	PE_SOC_TX_C_DP14	109	GND
95	PE_SOC_RX_DN14	110	GND
96	PE_SOC_TX_C_DN14	111	DISCONN_A2_EN
97	GND	112	P3V3_S
98	GND	113	DISCONN_A3_EN
99	PE_SOC_RX_DP15	114	P3V3_S
100	PE_SOC_TX_C_DP15	115	GND
101	PE_SOC_RX_DN15	116	GND
102	PE_SOC_TX_C_DN15	117	BYPASS_SLOT_EN
103	GND	118	P3V3_S
104	GND	119	BYPASS_SLOT_A
105	CLK_PCIE_SLOT_P	120	P3V3_S

Pin	Definition	Pin	Definition
121	GND	136	P12V_S2
122	GND	137	N.C.
123	BYPASS_SLOT_B	138	P12V_S2
124	P3V3_AUX	139	N.C.
125	BYPASS_SLOT_C	140	GND
126	P3V3_AUX	141	N.C.
127	GND	142	P12V_S2
128	GND	143	N.C.
129	BYPASS_SLOT_D	144	P12V_S2
130	P12V_S2	145	N.C.
131	N.C.	146	GND
132	P12V_S2	147	N.C.
133	N.C.	148	N.C.
134	GND	149	N.C.
135	N.C.	150	N.C.

Board to Board Connector (High Speed)

Connector size: 150 Pin, 0.8mm
Connector location: J6



Pin	Definition	Pin	Definition
1	GND	16	USB_0_OC#
2	GND	17	SMB_HOST_DATA
3	P12V2	18	CLK_32K_SUSCLK_SOC
4	P3V3_S	19	GND
5	P12V2	20	GND
6	P3V3_S	21	SW_INIT_DONE
7	GND	22	SW_UART_RXD
8	GND	23	TEMP_INT_N
9	P12V2	24	SW_UART_TXD
10	P12V_AUX	25	GND
11	P12V2	26	GND
12	P12V_AUX	27	3258_MR_N
13	GND	28	PMD_L0_RX_P
14	GND	29	RESETN1
15	SMB_HOST_CLK	30	PMD_L0_RX_N

Pin	Definition	Pin	Definition
31	GND	46	PMD_L3_RX_P
32	GND	47	CR0_TX_DN1
33	SYSRST_OUT_N	48	PMD_L3_RX_N
34	PMD_L1_RX_P	49	GND
35	RST_M_RESET_N	50	GND
36	PMD_L1_RX_N	51	CR0_TX_DP2
37	GND	52	3258_L0_RX_P_C
38	GND	53	CR0_TX_DN2
39	CR0_TX_DP0	54	3258_L0_RX_N_C
40	PMD_L2_RX_P	55	GND
41	CR0_TX_DN0	56	GND
42	PMD_L2_RX_N	57	CR0_TX_DP3
43	GND	58	3258_L1_RX_P_C
44	GND	59	CR0_TX_DN3
45	CR0_TX_DP1	60	3258_L1_RX_N_C

Pin	Definition	Pin	Definition
61	GND	76	5G_LTE_TX_DP0_C
62	GND	77	3258_L2_TX_N
63	3258_L0_TX_P	78	5G_LTE_TX_DN0_C
64	3258_L2_RX_P_C	79	GND
65	3258_L0_TX_N	80	GND
66	3258_L2_RX_N_C	81	3258_L3_TX_P
67	GND	82	5G_LTE_TX_DP1_C
68	GND	83	3258_L3_TX_N
69	3258_L1_TX_P	84	5G_LTE_TX_DN1_C
70	3258_L3_RX_P_C	85	GND
71	3258_L1_TX_N	86	GND
72	3258_L3_RX_N_C	87	CLK_OUT_DP6
73	GND	88	5G_LTE_TX_DP2_C
74	GND	89	CLK_OUT_DN6
75	3258_L2_TX_P	90	5G_LTE_TX_DN2_C

Pin	Definition	Pin	Definition
91	GND	106	5G_LTE_RX_DP1
92	GND	107	SMB_GBE1_I2C_DATA_R
93	CLK_OUT_DP7	108	5G_LTE_RX_DN1
94	USB3_TX_P1_C	109	GND
95	CLK_OUT_DN7	110	GND
96	USB3_TX_N1_C	111	SMB_GBE2_I2C_CLK_R
97	GND	112	5G_LTE_RX_DP2
98	GND	113	SMB_GBE2_I2C_DATA_R
99	SMB_GBE0_I2C_CLK_R	114	5G_LTE_RX_DN2
100	5G_LTE_RX_DP0_C	115	GND
101	SMB_GBE0_I2C_DATA_R	116	GND
102	5G_LTE_RX_DN0_C	117	SMB_GBE3_I2C_CLK_R
103	GND	118	USB3_RX_P1_C
104	GND	119	SMB_GBE3_I2C_DATA_R
105	SMB_GBE1_I2C_CLK_R	120	USB3_RX_N1_C

Pin	Definition	Pin	Definition
121	GND	136	SMB_ETH_MNG_I2C_CLK_R
122	GND	137	PD_GBE_GPIO5_R
123	SMB_CPLD_I2C_CLK_R	138	SMB_ETH_MNG_I2C_DATA_R
124	PEX_SW_RX_P	139	GND
125	SMB_CPLD_I2C_DATA_R	140	GND
126	PEX_SW_RX_N	141	FM_GBE_GPIO2_PRSNT_3_ N_R
127	GND	142	RST_SW_LTB_RSTBTN_N
128	GND	143	RST_GBE_GPIO3_RST_1_N_R
129	RST_GBE_GPIO6_RST_0_N_R	144	FM_SW_LTB_PWRBTN_N
130	PEX_SW_TX_P_C	145	GND
131	FM_GBE_GPIO7_INT_0_N_R	146	GND
132	PEX_SW_TX_N_C	147	RST_GBE_GPIO0_RST_3_N_R
133	GND	148	CLK_100M_SW_DP
134	GND	149	FM_GBE_GPIO1_INT_3_N_R
135	FM_GBE_GPIO4_INT_1_N_R	150	CLK_100M_SW_DN

Core Power PWM SMBus Header

Connector size: 1 x 3 = 3 pin, 2.54mm
Connector location: JP21*

Pin	Definition
1	PVCCIN_SCL
2	PVCCIN_SDA
3	GND

NAC Power PWM SMBus Header

Connector size: 1 x 3 = 3 pin, 2.54mm
Connector location: JP22*

Pin	Definition
1	PVNN_NAC_SCL
2	PVNN_NAC_SDA
3	GND

These headers are designed to update VCCIN, PVNN_PCH PM ICs using a tool.

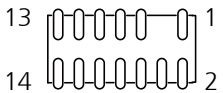
CPLD JTAG Header

Connector size: 1 x 6 = 6 pin, 2.54mm
Connector location: JP26

Pin	Definition
1	P3V3_AUX
2	GND
3	JTAG_PLD_TCK
4	JTAG_PLD_TDO
5	JTAG_PLD_TDI
6	JTAG_PLD_TMS

LPC TPM Module Header

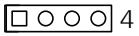
Connector size: 2 x 7 = 14 pin, 2.0mm
Connector location: JP34



Pin	Definition	Pin	Definition
1	GND	2	CLK_LPC_TPM
3	-	4	H_LPC_FRAME_N
5	ESPI_IO3_LPC_AD2	6	RST_TPM_N
7	ESPI_IO3_LPC_AD1	8	ESPI_IO3_LPC_AD3
9	GND	10	ESPI_IO3_LPC_AD0
11	INT_SERIRQ	12	P3V3_SOC
13	GND	14	GND

CPLD JTAG Header

Connector size: 1 x 4 = 4 pin, 2.54mm
Connector location: JP35

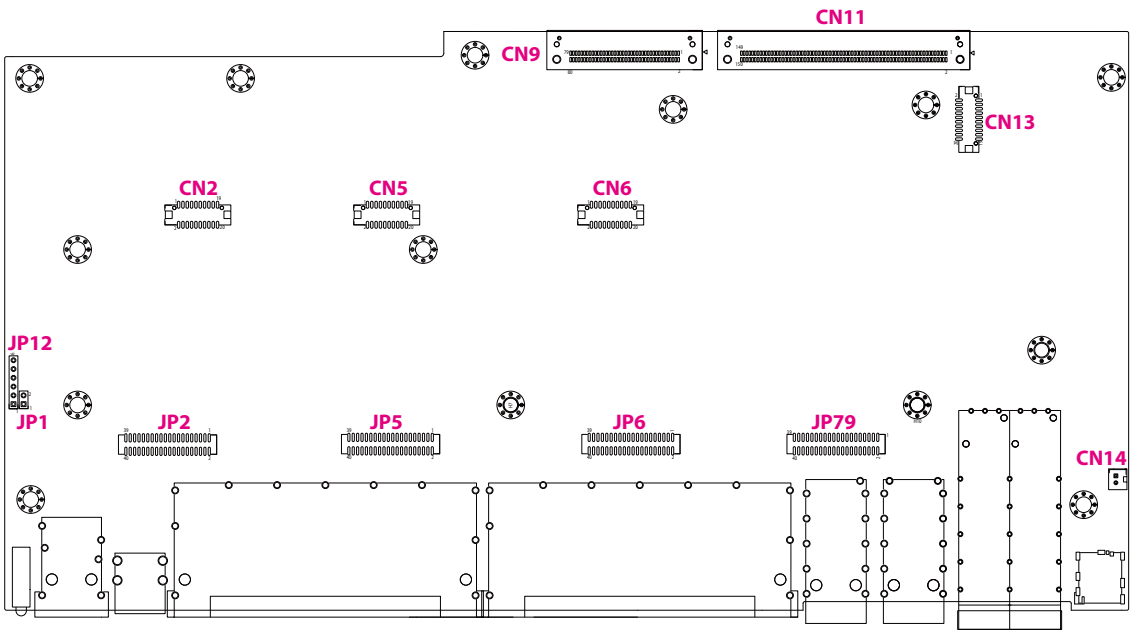


Pin	Definition
1	P3V3_AUX
2	BMC_CPLD_DEBUG_RXD
5	BMC_CPLD_DEBUG_TXD
6	GND

Locations of the Extension Board Connectors

The following figures show the extension board used in the FTA 1170, and indicates the locations of the connectors. Refer to this section for detailed pin settings and definitions of the connectors marked in pink on the figure below.

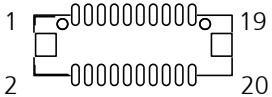
FTA 1170 Extension Board Top View



Connector Pin Definitions

PoE Power Connector (only 54V supply)

Connector type: 2 x 10 = 20 Pin, 1.25mm
Connector location: CN2, CN5, CN6, CN13



CN2 (For Marvell 2.5GBE Phy1)

Pin	Definition	Pin	Definition
1	N.C.	11	POE2_ADDR0
2	N.C.	12	N.C.
3	N.C.	13	POE2_ADDR1
4	N.C.	14	N.C.
5	N.C.	15	POE2_ADDR2
6	N.C.	16	N.C.
7	N.C.	17	N.C.
8	N.C.	18	N.C.
9	V_3P3V_POE_MOD2	19	GND_POE2
10	V_3P3V_POE_MOD2	20	N.C.

CN5 (For Marvell 2.5GBE Phy2)

Pin	Definition	Pin	Definition
1	N.C.	11	POE3_ADDR0
2	N.C.	12	N.C.
3	N.C.	13	POE3_ADDR1
4	N.C.	14	N.C.
5	N.C.	15	POE3_ADDR2
6	N.C.	16	N.C.
7	N.C.	17	N.C.
8	N.C.	18	N.C.
9	V_3P3V_POE_MOD3	19	GND_POE3
10	V_3P3V_POE_MOD3	20	N.C.

CN6 (For Marvell 2.5GBE Phy3)

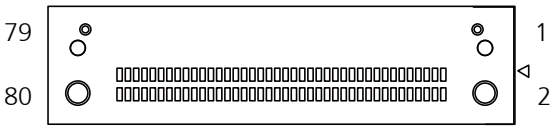
Pin	Definition	Pin	Definition
1	N.C.	11	POE1_ADDR0
2	N.C.	12	N.C.
3	N.C.	13	POE1_ADDR1
4	N.C.	14	N.C.
5	N.C.	15	POE1_ADDR2
6	N.C.	16	N.C.
7	N.C.	17	N.C.
8	N.C.	18	N.C.
9	V_3P3V_POE_MOD1	19	GND_POE1
10	V_3P3V_POE_MOD1	20	N.C.

CN13 (For X557 10GBE)

Pin	Definition	Pin	Definition
1	N.C.	11	POE4_ADDR0
2	N.C.	12	N.C.
3	N.C.	13	POE4_ADDR1
4	N.C.	14	N.C.
5	N.C.	15	POE4_ADDR2
6	N.C.	16	N.C.
7	N.C.	17	N.C.
8	N.C.	18	N.C.
9	V_3P3V_POE_MOD4	19	GND_POE4
10	V_3P3V_POE_MOD4	20	N.C.

Board to Board Connector (Low Speed)

Connector type: 80 Pin, 0.8mm
Connector location: CN9



Pin	Definition	Pin	Definition
1	BMC_CPLD_RI_N	11	BMC_CPLD_DTR_N
2	FM_SOC_CPLD_SLP_S3_N	12	GND
3	BMC_CPLD_RXD	13	BMC_CPLD_TXD
4	N.C.	14	USB2_P0_DN
5	BMC_CPLD_DSR_N	15	BMC_CPLD_RTS_N
6	N.C.	16	USB2_P0_DP
7	BMC_CPLD_CTS_N	17	PU_NIC0_NCSI_RXD_1
8	IRQ_5GM2_WAKE_N	18	GND
9	BMC_CPLD_DCD_N	19	PD_NIC0_NCSI_CRS_DV
10	MB_ ATX_PWROK	20	USB2_P1_DN

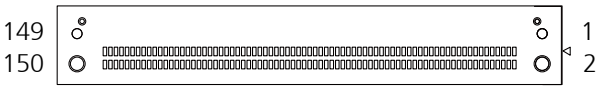
Pin	Definition	Pin	Definition
21	NIC0_NCSI_CLK_IN_R	31	FM_NIC0_DISABLE_N
22	USB2_P1_DP	32	USB3_TX_N0
23	PU_NIC0_NCSI_RXD_0	33	IRQ_NIC0_WAKE
24	GND	34	USB3_TX_P0
25	PU_NIC0_NCSI_TXD_0	35	RST_CPLD_NIC1_RESET_ N_R
26	USB3_RX_N0	36	GND
27	PU_NIC0_NCSI_TXD_1	37	SMB_NIC0_ALERT_N
28	USB3_RX_P0	38	LED_GBE0_LED0
29	PD_NIC0_NCSI_TX_EN	39	GND
30	GND	40	LED_GBE0_LED1

Pin	Definition	Pin	Definition
41	SMB_NIC0_CLK	51	LED_GBE1_LED2
42	GND	52	P1E_NIC0_RX_DP
43	SMB_NIC0_DAT	53	LED_GBE2_LED0
44	CLK_100M_NIC0_DN_R	54	GND
45	LED_GBE0_LED2	55	LED_GBE2_LED1
46	CLK_100M_NIC0_DP_R	56	P1E_NIC0_TX_C_DN
47	LED_GBE1_LED0	57	LED_GBE2_LED2
48	GND	58	P1E_NIC0_TX_C_DP
49	LED_GBE1_LED1	59	LED_GBE3_LED0
50	P1E_NIC0_RX_DN	60	GND

Pin	Definition	Pin	Definition
61	LED_GBE3_LED1	71	POWER_LED
62	GND	72	P3V3_MB
63	LED_GBE3_LED2	73	GND
64	P3V3_AUX	74	GND
65	POE_LED	75	P12V
66	P3V3_AUX	76	P3V3_MB
67	WIFI_LED	77	P12V
68	GND	78	P3V3_MB
69	HDD_CPLD_LED	79	GND
70	P3V3_MB	80	GND

Board to Board Connector (High Speed)

Connector size: 150 Pin, 0.8mm
Connector location: CN11



Pin	Definition	Pin	Definition
1	GND	16	USB_0_OC#
2	GND	17	SMB_HOST_DATA
3	P12V	18	CLK_32K_SUSCLK_SOC
4	P3V3_MB	19	GND
5	P12V	20	GND
6	P3V3_MB	21	SW_INIT_DONE_R
7	GND	22	SW_UART_RXD
8	GND	23	TEMP_INT_N_R
9	P12V	24	SW_UART_TXD
10	P12V_AUX	25	GND
11	P12V	26	GND
12	P12V_AUX	27	3258_MR_N
13	GND	28	PMD_L0_RX_P
14	GND	29	RESETN1_R
15	SMB_HOST_CLK	30	PMD_L0_RX_N

Pin	Definition	Pin	Definition
31	GND	46	PMD_L3_RX_P
32	GND	47	PMD_L1_TX_N
33	SYSRST_OUT_N_R	48	PMD_L3_RX_N
34	PMD_L1_RX_P	49	GND
35	RST_M_RESET_N_R	50	GND
36	PMD_L1_RX_N	51	PMD_L2_TX_P
37	GND	52	3258_L0_RX_P
38	GND	53	PMD_L2_TX_N
39	PMD_L0_TX_P	54	3258_L0_RX_N
40	PMD_L2_RX_P	55	GND
41	PMD_L0_TX_N	56	GND
42	PMD_L2_RX_N	57	PMD_L3_TX_P
43	GND	58	3258_L1_RX_P
44	GND	59	PMD_L3_TX_N
45	PMD_L1_TX_P	60	3258_L1_RX_N

Pin	Definition	Pin	Definition
61	GND	76	N.C.
62	GND	77	88X3310P_L0_TX_N
63	3258_L0_TX_P	78	N.C.
64	88X3310P_L0_RX_P	79	GND
65	3258_L0_TX_N	80	GND
66	88X3310P_L0_RX_N	81	88X3310P_L1_TX_P
67	GND	82	5G_LTE_TX_DP1
68	GND	83	88X3310P_L1_TX_N
69	3258_L1_TX_P	84	5G_LTE_TX_DN1
70	88X3310P_L1_RX_P	85	GND
71	3258_L1_TX_N	86	GND
72	88X3310P_L1_RX_N	87	CLK_OUT_DP6
73	GND	88	5G_LTE_TX_DP2
74	GND	89	CLK_OUT_DN6
75	88X3310P_L0_TX_P	90	5G_LTE_TX_DN2

Pin	Definition	Pin	Definition
91	GND	106	5G_LTE_RX_DP1
92	GND	107	TP_SMB_GBE1_I2C_DATA
93	CLK_OUT_DP7	108	5G_LTE_RX_DN1
94	USB3_TX_P1	109	GND
95	CLK_OUT_DN7	110	GND
96	USB3_TX_N1	111	TP_SMB_GBE2_I2C_CLK
97	GND	112	5G_LTE_RX_DP2
98	GND	113	TP_SMB_GBE2_I2C_DATA
99	SMB_GBE0_I2C_CLK	114	5G_LTE_RX_DN2
100	N.C.	115	GND
101	SMB_GBE0_I2C_DATA	116	GND
102	N.C.	117	TP_SMB_GBE3_I2C_CLK
103	GND	118	USB3_RX_P1
104	GND	119	TP_SMB_GBE3_I2C_DATA
105	TP_SMB_GBE1_I2C_CLK	120	USB3_RX_N1

Pin	Definition	Pin	Definition
121	GND	136	X557_MDC_SCL
122	GND	137	PD_GBE_GPIO5_R
123	SMB_CPLD_I2C_CLK_R	138	X557_MDIO_SDA
124	PEX_SW_RX_P_C	139	GND
125	SMB_CPLD_I2C_DATA_R	140	GND
126	PEX_SW_RX_N_C	141	FM_GBE_GPIO2_ PRSNT_3_ N_R
127	GND	142	RST_SW_LTB_RSTBTN_N
128	GND	143	RST_GBE_GPIO3_RST_1_ N_R
129	RST_GBE_GPIO6_RST_0_ N_R	144	FM_SW_LTB_PWRBTN_N
130	PEX_SW_TX_P	145	GND
131	FM_GBE_GPIO7_INT_0_N_ R	146	GND
132	PEX_SW_TX_N	147	RST_GBE_GPIO0_RST_3_ N_R
133	GND	148	CLK_100M_SW_DP_R
134	GND	149	FM_GBE_GPIO1_INT_3_N_ R
135	FM_GBE_GPIO4_INT_1_N_ R	150	CLK_100M_SW_DN_R

Reset Button Header

Connector size: 1 x 2 = 2 Pin, 2.0mm
Connector location: CN14

Pin	Definition
1	FP_RST_BTN_N_R
2	GND

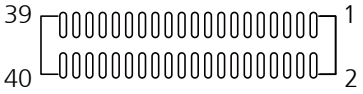
Power Button Header

Connector size: 1 x 2 = 2 Pin, 2.54mm
Connector location: JP1

Pin	Definition
1	PWRBTN#_C
2	GND

PoE Box Header (Connector to PoE module)

Connector type: 2 x 20 = 40 Pin, 1.27mm
Connector location: JP2, JP5, JP6, JP79



JP2 (for Marvell 2.5GBE RJ45 P1~P8 PoE)

Pin	Definition	Pin	Definition
1	N.C.	11	N.C.
2	VPORT_NEG_OUT4	12	N.C.
3	N.C.	13	P12V
4	N.C.	14	VPORT_NEG_OUT1
5	N.C.	15	GND
6	VPORT_NEG_OUT3	16	V_52V_OUT
7	N.C.	17	P3V3
8	N.C.	18	V_52V_OUT
9	N.C.	19	P3V3
10	VPORT_NEG_OUT2	20	V_52V_OUT

Pin	Definition	Pin	Definition
21	GND	31	DRG_SPI_MOSI
22	V_52V_OUT	32	VPORT_NEG_OUT7
23	POE1_DETECT	33	GND
24	V_52V_OUT	34	N.C.
25	GND	35	DRG_SPI_SCK
26	V_52V_OUT	36	VPORT_NEG_OUT6
27	DRG_SPI_MISO	37	GND
28	VPORT_NEG_OUT8	38	N.C.
29	GND	39	DRG_SPI_CS
30	N.C.	40	VPORT_NEG_OUT5

JP5 (for Marvell 2.5GBE RJ45 P9~P16 PoE)

Pin	Definition	Pin	Definition
1	N.C.	11	N.C.
2	VPORT_NEG_OUT12	12	N.C.
3	N.C.	13	P12V
4	N.C.	14	VPORT_NEG_OUT9
5	N.C.	15	GND
6	VPORT_NEG_OUT11	16	V_52V_OUT
7	N.C.	17	P3V3
8	N.C.	18	V_52V_OUT
9	N.C.	19	P3V3
10	VPORT_NEG_OUT10	20	V_52V_OUT

Pin	Definition	Pin	Definition
21	GND	31	DRG_SPI_MOSI
22	V_52V_OUT	32	VPORT_NEG_OUT15
23	POE2_DETECT	33	GND
24	V_52V_OUT	34	N.C.
25	GND	35	DRG_SPI_SCK
26	V_52V_OUT	36	VPORT_NEG_OUT14
27	DRG_SPI_MISO	37	GND
28	VPORT_NEG_OUT16	38	N.C.
29	GND	39	DRG_SPI_CS
30	N.C.	40	VPORT_NEG_OUT13

JP6 (for Marvell 2.5GBE RJ45 P17~P24 PoE)

Pin	Definition	Pin	Definition
1	N.C.	11	N.C.
2	VPORT_NEG_OUT20	12	N.C.
3	N.C.	13	P12V
4	N.C.	14	VPORT_NEG_OUT17
5	N.C.	15	GND
6	VPORT_NEG_OUT19	16	V_52V_OUT
7	N.C.	17	P3V3
8	N.C.	18	V_52V_OUT
9	N.C.	19	P3V3
10	VPORT_NEG_OUT18	20	V_52V_OUT

Pin	Definition	Pin	Definition
21	GND	31	DRG_SPI_MOSI
22	V_52V_OUT	32	VPORT_NEG_OUT23
23	POE3_DETECT	33	GND
24	V_52V_OUT	34	N.C.
25	GND	35	DRG_SPI_SCK
26	V_52V_OUT	36	VPORT_NEG_OUT22
27	DRG_SPI_MISO	37	GND
28	VPORT_NEG_OUT24	38	N.C.
29	GND	39	DRG_SPI_CS
30	N.C.	40	VPORT_NEG_OUT21

JP79 (for Intel X557 10GBE RJ45 P1~P4 PoE)

Pin	Definition	Pin	Definition
1	N.C.	11	N.C.
2	VPORT_NEG_10G_OUT4	12	N.C.
3	N.C.	13	P12V
4	N.C.	14	VPORT_NEG_10G_OUT1
5	N.C.	15	GND
6	VPORT_NEG_10G_OUT3	16	V_52V_OUT
7	N.C.	17	P3V3
8	N.C.	18	V_52V_OUT
9	N.C.	19	P3V3
10	VPORT_NEG_10G_OUT2	20	V_52V_OUT

Pin	Definition	Pin	Definition
21	GND	31	DRG_SPI_MOSI
22	V_52V_OUT	32	VPORT_NEG_10G_OUT7
23	POE4_DETECT	33	GND
24	V_52V_OUT	34	N.C.
25	GND	35	DRG_SPI_SCK
26	V_52V_OUT	36	VPORT_NEG_10G_OUT6
27	DRG_SPI_MISO	37	GND
28	VPORT_NEG_10G_OUT8	38	N.C.
29	GND	39	DRG_SPI_CS
30	N.C.	40	VPORT_NEG_10G_OUT5

I/O Board CPLD JTAG Header

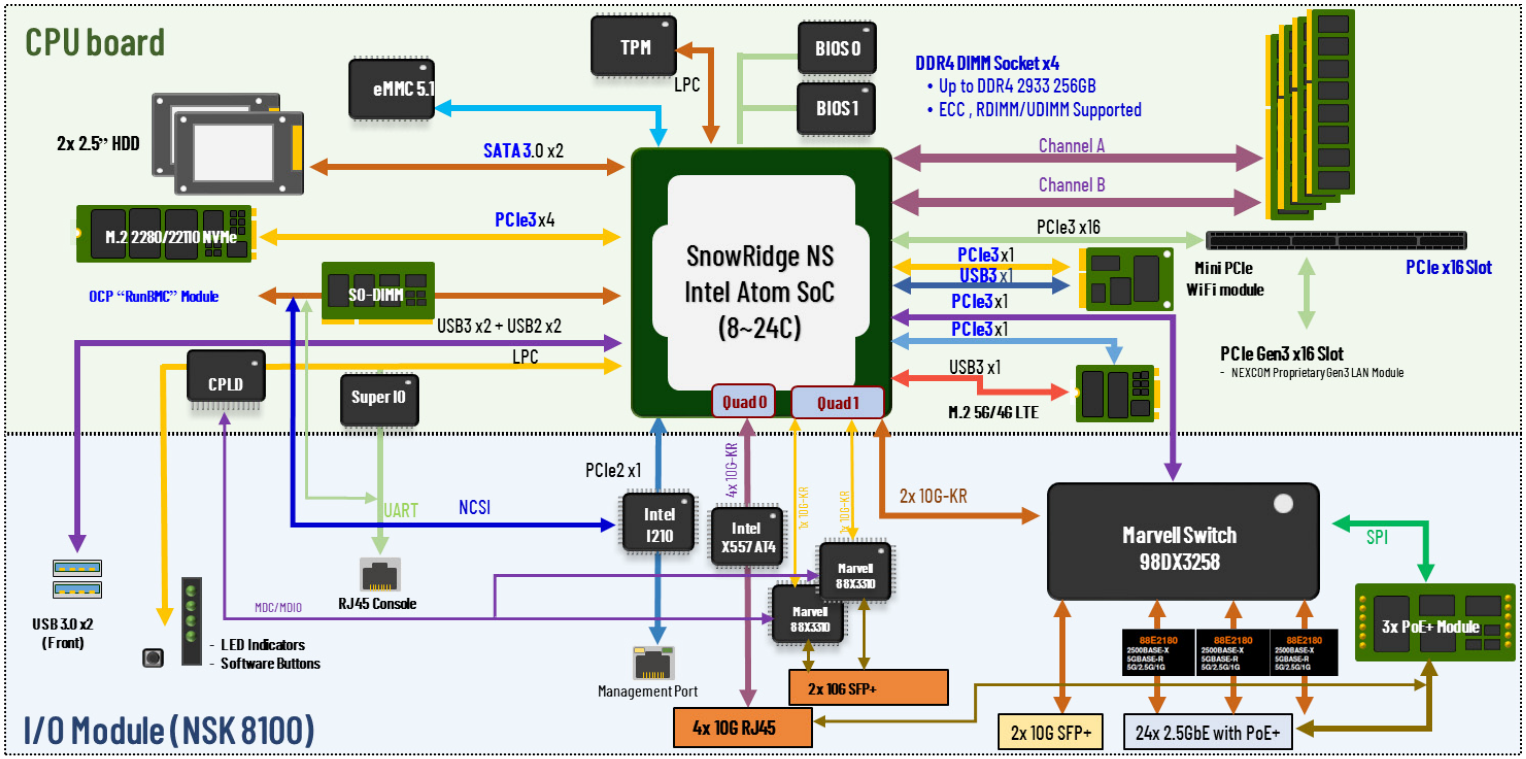
Connector size: 1 x 6 = 6 Pin , 2.54mm
Connector location: JP12

Pin	Definition
1	P3V3_AUX
2	GND
3	JTAG_CPLD_TCK
4	JTAG_CPLD_TDO
5	JTAG_CPLD_TDI
6	JTAG_CPLD_TMS

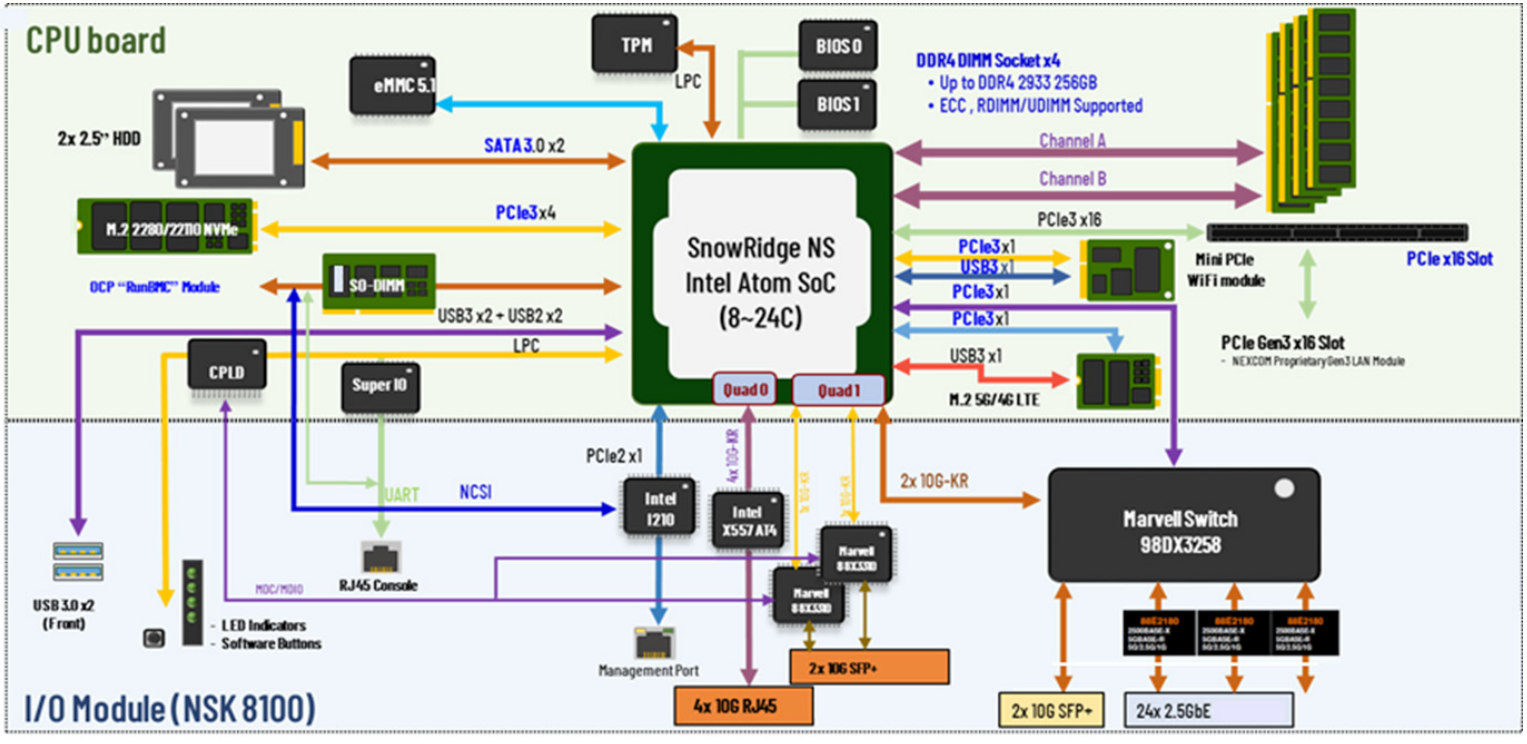
This header is designed to update CPLD firmware with a diamond programmer.

Block Diagram

FTA1170



FTA1170A



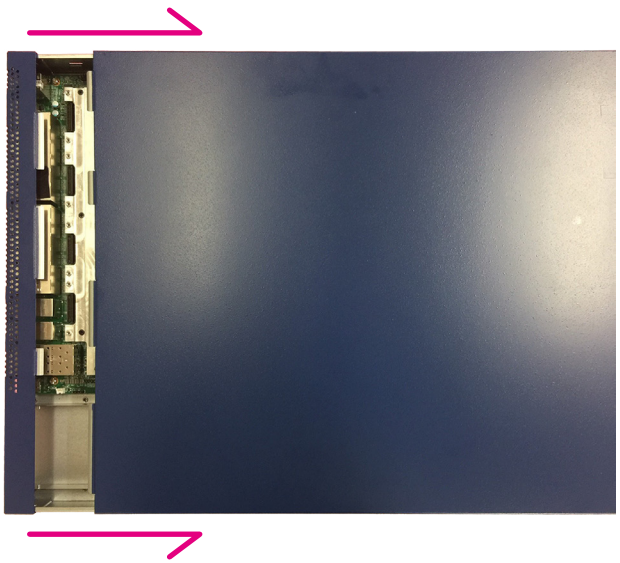
Chapter 3: System Setup

Removing the Chassis Cover

Prior to removing the chassis cover, make sure the unit's power is off and disconnected from the power sources for 20 seconds to prevent electric shock or system damage.

1. The screws located on the rear panel and used to secure the cover to the chassis. Remove these screws and put them in a safe place for later use.

2. With the screws removed, gently slide the cover outwards and then lift up the cover to remove it.

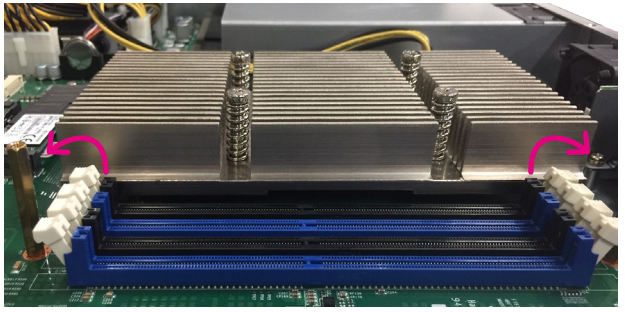


Installing Memory Modules

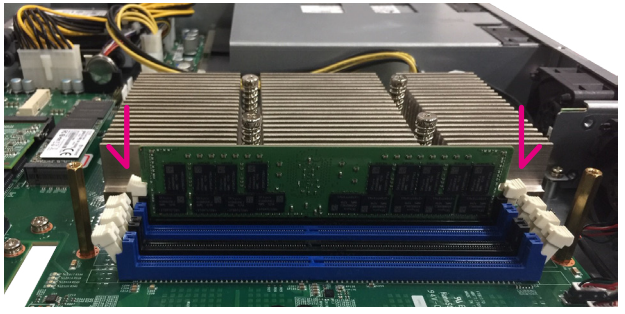
Before beginning the memory installation, please pay attention to the following notices.

- Before installing or removing internal components on the motherboard, please ensure that the AC power cord is unplugged for at least over 20 seconds.
- The memory modules are foolproof design and can only be installed in one direction. If you encounter difficulty, try reversing the module's orientation and avoid using force to prevent damage.
- It is recommended to install memory modules with the same brand, speed, and capacity.
- To install a single memory module, it is recommended to plug the module into the A1 slot. For dual-channel installation, the sequence should be A1 and B1, followed by A0 and B0. Refer to Chapter 2 for the mechanical location and sequence of DIMM slots.

1. Locate the DIMM slots on the motherboard and release the locks.

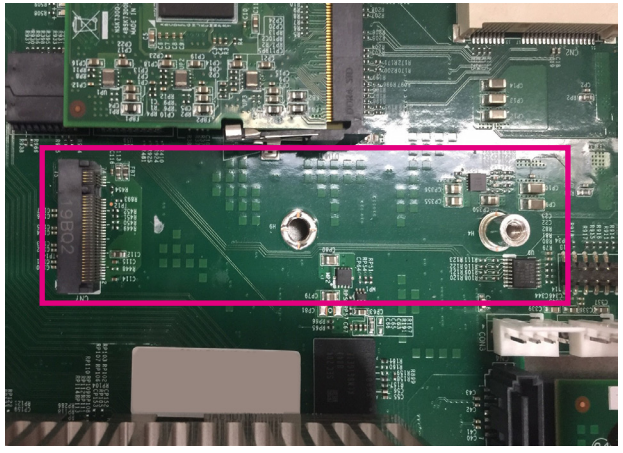


2. Insert the modules into the sockets at a 90 degree angle. Apply firm, even pressure to both ends of the modules until they slip into the sockets.

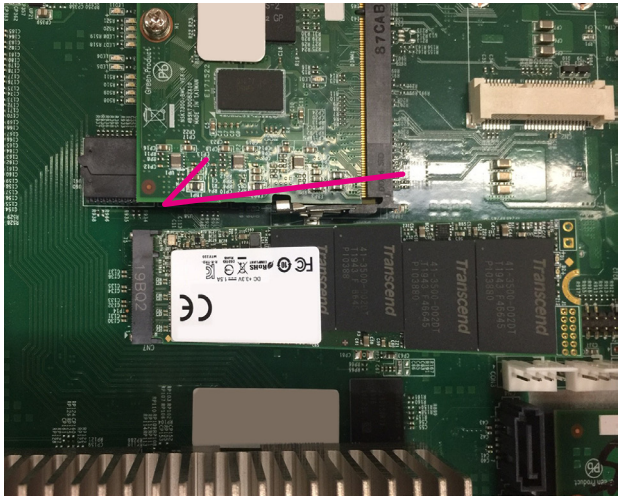


Installing an M.2 Key M Storage Device

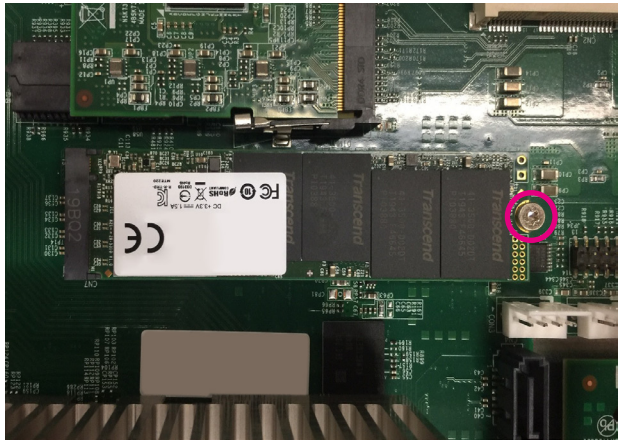
1. Locate the M.2 slot on the motherboard.



2. Insert the M.2 SSD into the M.2 slot at a 45 degree angle until the gold -plated connector on the edge of the module completely disappears inside the slot.

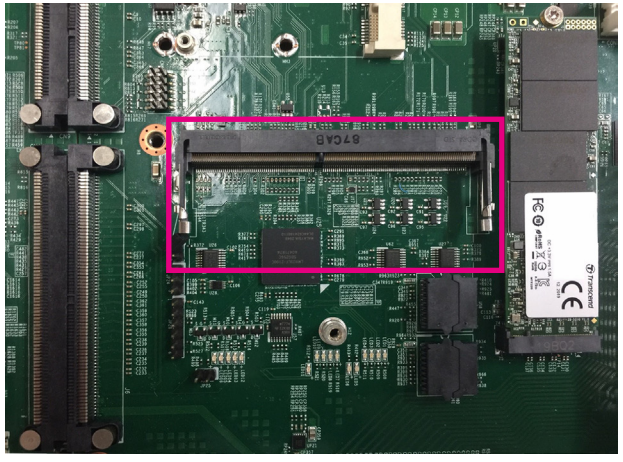


3. With the module fully inserted, tighten a screw into the mounting hole on the module to secure it.

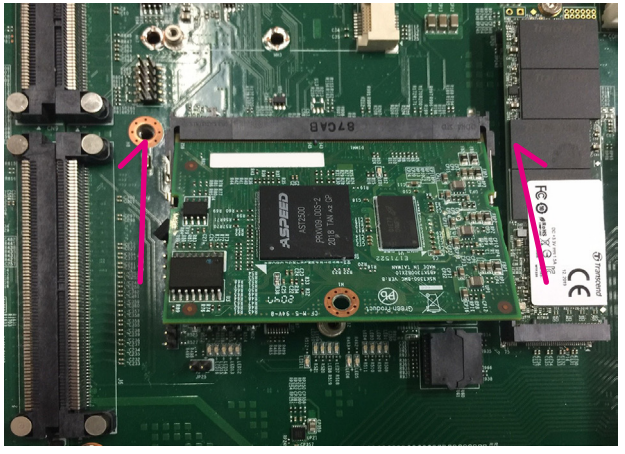


Installing a BMC Module

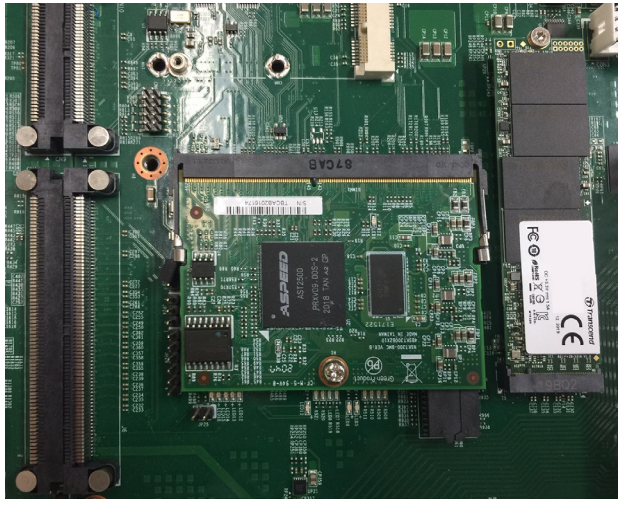
1. Locate the BMC socket on the motherboard.



2. Insert the BMC module into the BMC socket at a 45 degree angle until the gold-plated connector on the edge of the module completely disappears inside the slot.

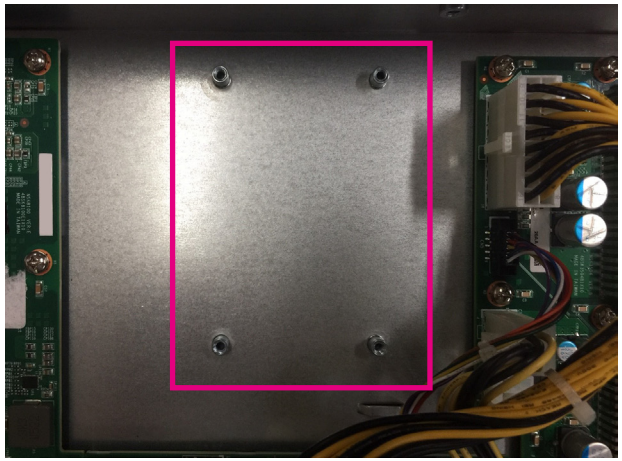


3. Push the module down until the clips on both sides of the socket lock into position. A distinctive "click" sound will indicate the module is correctly locked into place.



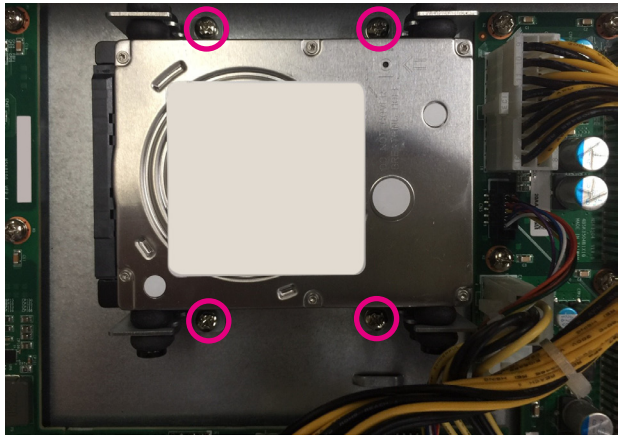
Installing a 2.5" SATA Hard Drive

1. Locate the HDD bracket, then unscrew and remove it from the chassis.

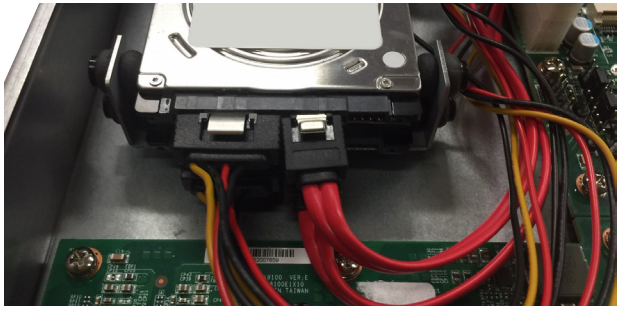


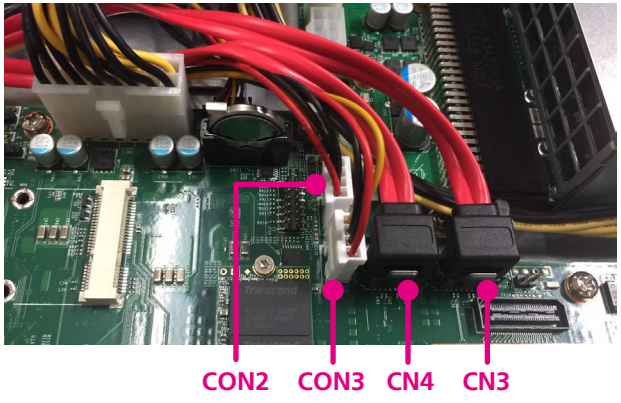
2. Tighten the hard drive with screws on both sides of the bracket. The bracket is designed to support the assembly of up to 2 hard drives.

3. Tighten the bracket with the installed hard drive(s) in the location from which it was previously removed on the chassis.



4. Connect the SATA data and power cables from the hard drive(s) to the motherboard.





Chapter 4: BIOS Setup

This chapter describes how to use the BIOS setup program for the FTA 1170 series. The BIOS screens provided in this chapter are for reference only and may change if the BIOS is updated in the future.

To check for the latest updates and revisions, visit the NEXCOM website at www.nexcom.com.tw.

About BIOS Setup

The BIOS (Basic Input and Output System) Setup program is a menu driven utility that enables you to make changes to the system configuration and tailor your system to suit your individual work needs. It is a ROM-based configuration utility that displays the system's configuration status and provides you with a tool to set system parameters.

These parameters are stored in non-volatile battery-backed-up CMOS RAM that saves this information even when the power is turned off. When the system is turned back on, the system is configured with the values found in CMOS.

With easy-to-use pull down menus, you can configure items such as:

- Hard drives, diskette drives, and peripherals
- Video display type and display options
- Password protection from unauthorized use
- Power management features

The settings made in the setup program affect how the computer performs. It is important, therefore, first to try to understand all the setup options, and second, to make settings appropriate for the way you use the computer.

When to Configure the BIOS

- This program should be executed under the following conditions:
- When changing the system configuration
- When a configuration error is detected by the system and you are prompted to make changes to the setup program
- When resetting the system clock
- When redefining the communication ports to prevent any conflicts
- When making changes to the Power Management configuration
- When changing the password or making other changes to the security setup

Normally, CMOS setup is needed when the system hardware is not consistent with the information contained in the CMOS RAM, whenever the CMOS RAM has lost power, or the system features need to be changed.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering Setup

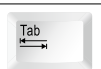
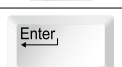
When the system is powered on, the BIOS will enter the Power-On Self Test (POST) routines. These routines perform various diagnostic checks; if an error is encountered, the error will be reported in one of two different ways:

- If the error occurs before the display device is initialized, a series of beeps will be transmitted.
- If the error occurs after the display device is initialized, the screen will display the error message.

Powering on the computer and immediately pressing 

allows you to enter Setup.

Legends

Key	Function
	Moves the highlight left or right to select a menu.
	Moves the highlight up or down between sub-menu or fields.
	Exits the BIOS Setup Utility.
	Scrolls forward through the values or options of the highlighted field.
	Scrolls backward through the values or options of the highlighted field.
	Selects a field.
	Displays General Help.
	Load previous values.
	Load optimized default values.
	Saves and exits the Setup program.
	Press <Enter> to enter the highlighted sub-menu

Scroll Bar

When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu

When "▶" appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press 

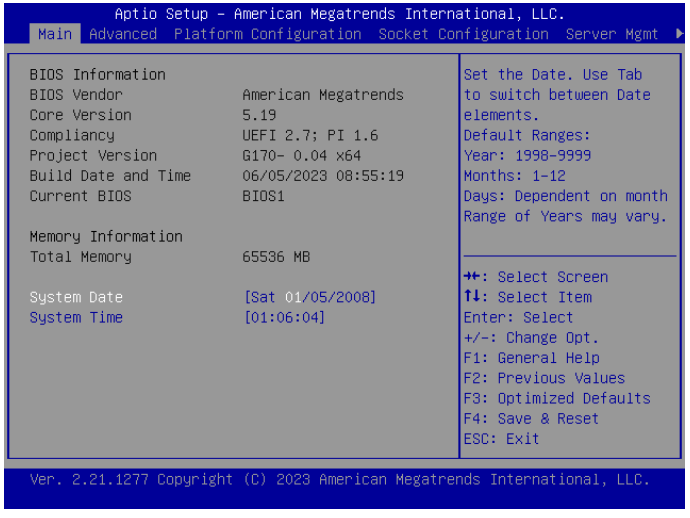
.

BIOS Setup Utility

Once you enter the AMI BIOS Setup Utility, the Main Menu will appear on the screen. The main menu allows you to select from several setup functions and one exit. Use arrow keys to select among the items and press Enter to accept or enter the submenu.

Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <day>, <month>, <date>, <year>. Day displays a day, from Monday to Sunday. Month displays the month, from 1 to 12. Date displays the date, from 1 to 31. Year displays the year, from 2005 to 2099.

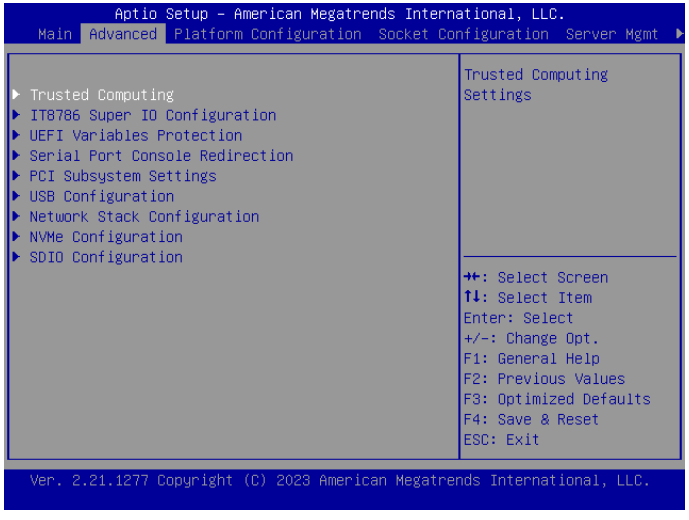
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

Advanced

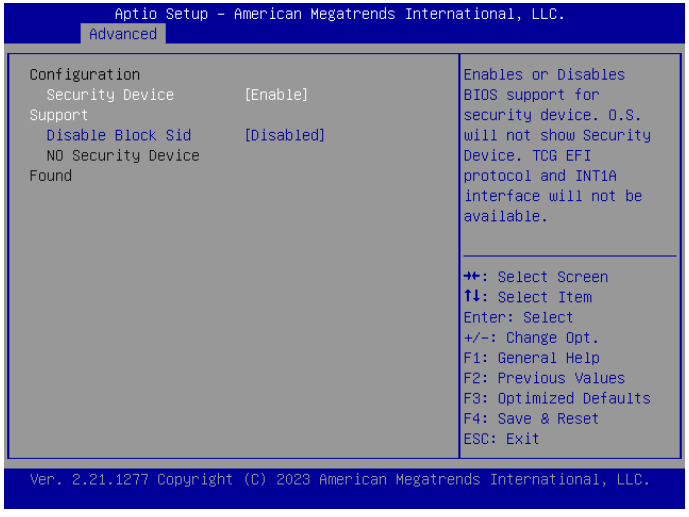
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Setting incorrect field values may cause the system to malfunction.



Trusted Computing

This section is used to configure Trusted Platform Module (TPM) settings.



Security Device Support

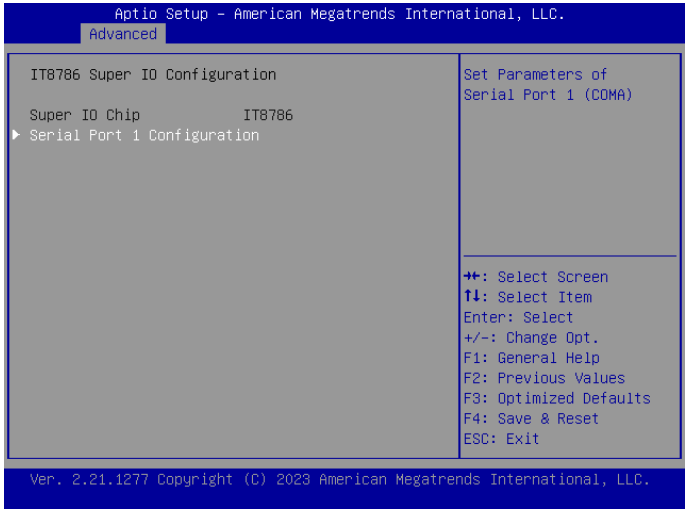
Enable or disable BIOS support for security device. O.S will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

Disable Block Sid

Override to allow SID authentication in TCG storage device.

IT8786 Super IO Configuration

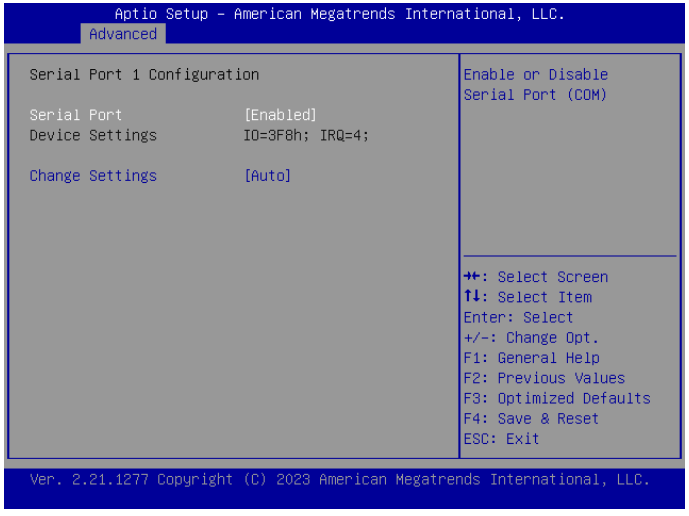
This section is used to configure the serial port of the super IO.



Super IO Chip
Display the super I/O chip used on the board.

Serial Port 1 Configuration
Enter Serial Port 1 Configuration submenu.

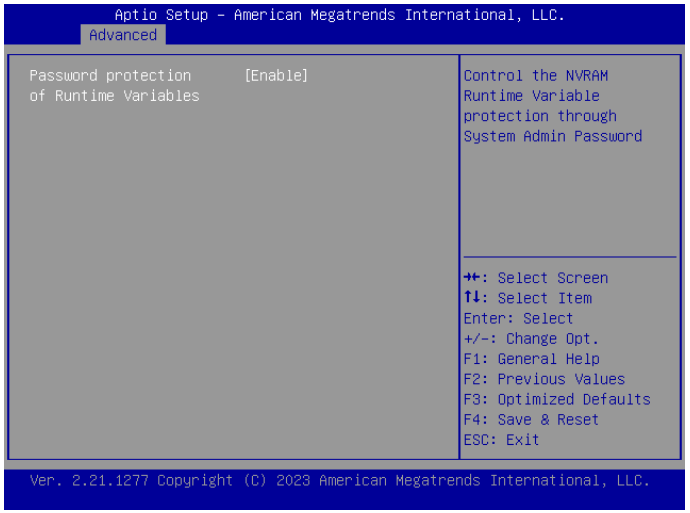
Serial Port 1 Configuration
This section is used to configure serial port 1.



Serial Port
Enable or disable the serial port.

Change Settings
Select an optimal setting for the Super IO device.

UEFI Variables Protection

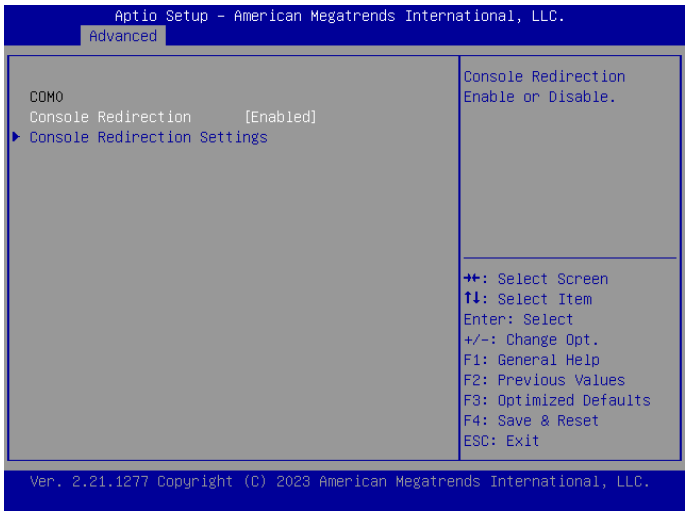


Password Protection of Runtime Variables

Control the NVRAM runtime variable protection through system admin password.

Serial Port Console Redirection

This section is used to configure the serial port that will be used for console redirection.



Console Redirection

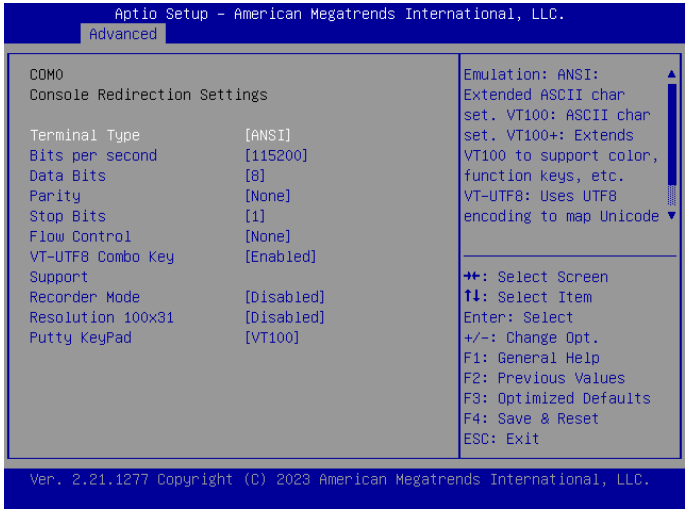
Enable or disable the console redirection.

Console Redirection Settings

When Console Redirection is enabled, Console Redirection Settings will be available.

Console Redirection Settings

This section is used to configure serial port 1.



Terminal Type

ANSI Extended ASCII character set.
VT100 ASCII character set.
VT100+ Extends VT100 to support color, function keys, etc.
VT-UTF8 Uses UTF8 encoding to map Unicode characters onto 1 or more bytes.

Bits Per Second

Selects the serial port transmission speed. The speed must match the other side. Long or noisy lines may require a lower speed.

Data Bits

The options are 7 and 8.

Parity

A parity bit can be sent with the data bits to detect some transmission errors.

Even Parity bit is 0 if the number of 1's in the data bits is even.
Odd Parity bit is 0 if number of 1's in the data bits is odd.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Flow Control

Flow control can prevent data loss from buffer overflow. When sending data and the receiving buffers are full, a "stop" signal can be sent to stop the data flow.

VT-UTF8 Combo Key Support

Enable or disable the VT-UTF8 combo key support.

Recorder Mode

When this field is enabled, only text will be sent. This is to capture the terminal data.

Resolution 100x31

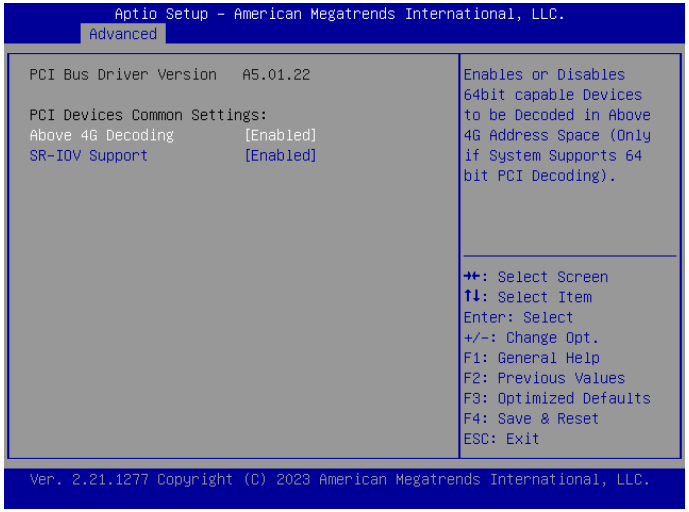
Enable or disable the extended terminal resolution.

Putty Keypad

Selects the Putty keyboard emulation type.

PCI Subsystem Settings

This section is used to configure the PCI.



Above 4G Decoding

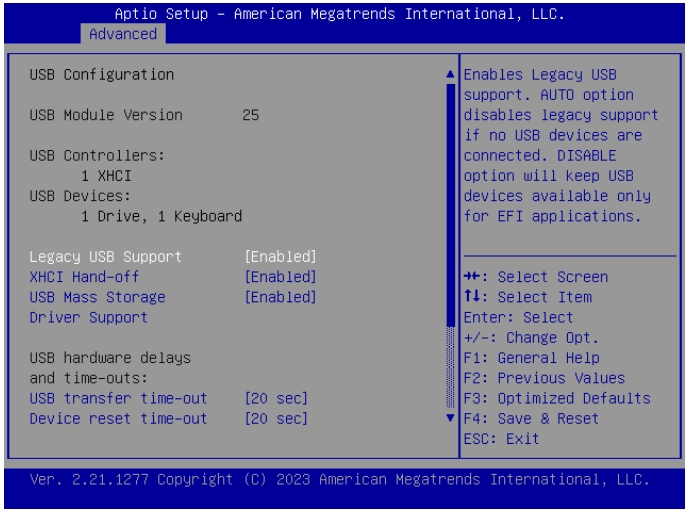
Enable or disable the decoding of 64-bit devices in 4G address space.

SR-IOV Support

Enable or disable the SR-IOV support.

USB Configuration

This section is used to configure the USB.



Legacy USB Support

Enable Enable Legacy USB.
Auto Disable support for Legacy when no USB devices are connected.
Disable Keep USB devices available only for EFI applications.

XHCI Hand-off

This is a workaround for OSes that does not support XHCI hand-off. The XHCI ownership change should be claimed by the XHCI driver.

USB Mass Storage Driver Support

Enable or disable the USB mass storage driver support.

USB Transfer Time-out

The time-out value for control, bulk, and Interrupt transfers.

Device Reset Time-out

Select the USB mass storage device's start unit command timeout.

Device Power-up Delay

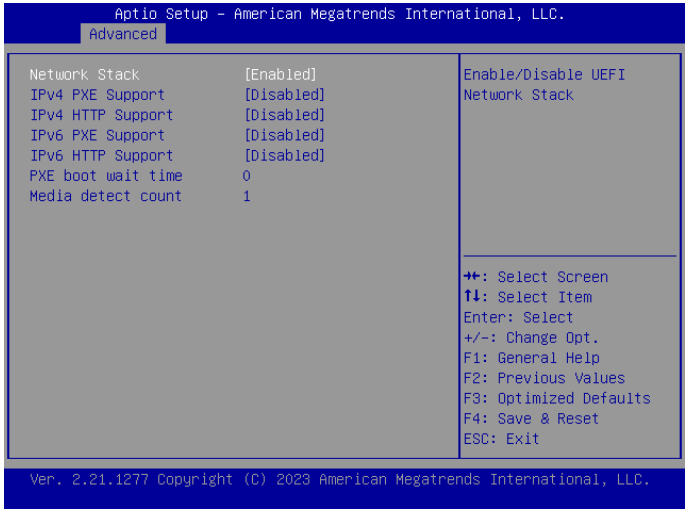
Maximum time the value will take before it properly reports itself to the Host Controller. "Auto" uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

Mass Storage Devices

Configure the mass storage device emulation type. AUTO enumerates devices according to their media format. Optical drives are emulated as CDROM, drives with no media will be emulated according to a drive type.

Network Stack Configuration

This section is used to configure the network stack.



Network Stack
Enable or disable the UEFI network stack. Once enabled, more options are available for configuration.

Ipv4 PXE Support
Enable or disable IPv4 PXE support. If disabled, the IPv4 boot option will not be created.

Ipv4 HTTP Support
Enable or disable Ipv4 HTTP support.

Ipv6 PXE Support
Enable or disable IPv6 PXE support. If disabled, the IPv6 boot option will not be created.

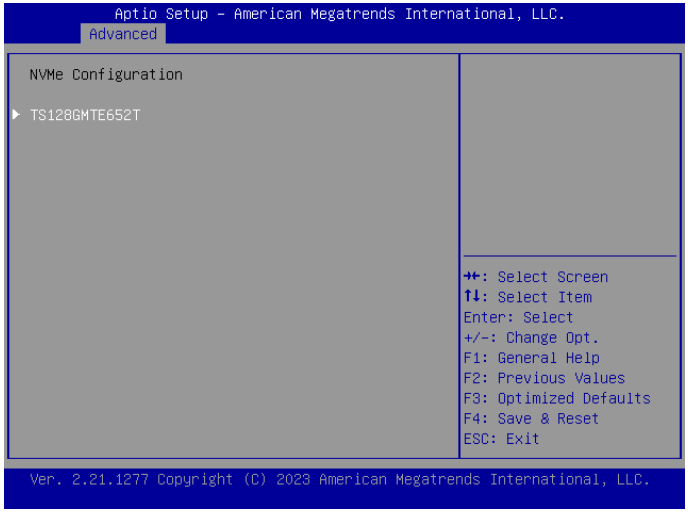
Ipv6 HTTP Support
Enable or disable Ipv6 HTTP support.

PXE boot wait time
Configure the wait time to press the ESC key to abort the PXE boot.

Media detect count
Configure the number of times the media will be checked.

NVMe Configuration

This section is used to configure the NVMe devices installed.

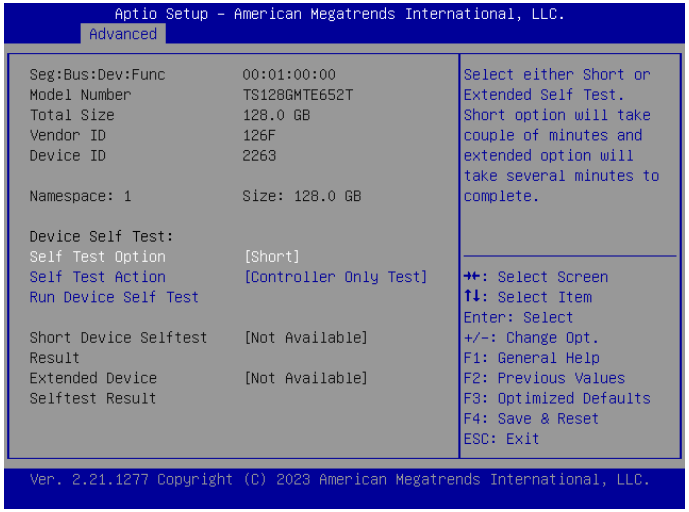


NVMe Device

Display the model of installed NVMe device. Press **Enter** for more advanced configurations.

NVMe Device Configuration

This section is used to configure the installed NVMe device.



Self Test Option

Configure the method used for self test.
Short: Short option will take couple of minutes to complete.
Extended: Extended option will take several minutes to complete.

Self Test Action

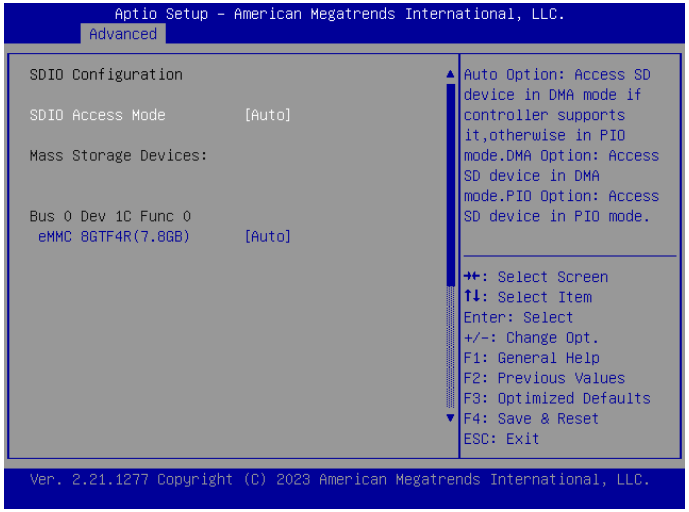
Configure the items used for self test. Controller Only Test and Controller and NameSpace Test options are available. Selecting Controller and NameSpace Test will take longer to complete.

Run Device Self Test

Run the device self test according to the self test option and action selected. Pressing the **Esc** key will abort the test.

SDIO Configuration

This section is used to configure the SDIO access mode.

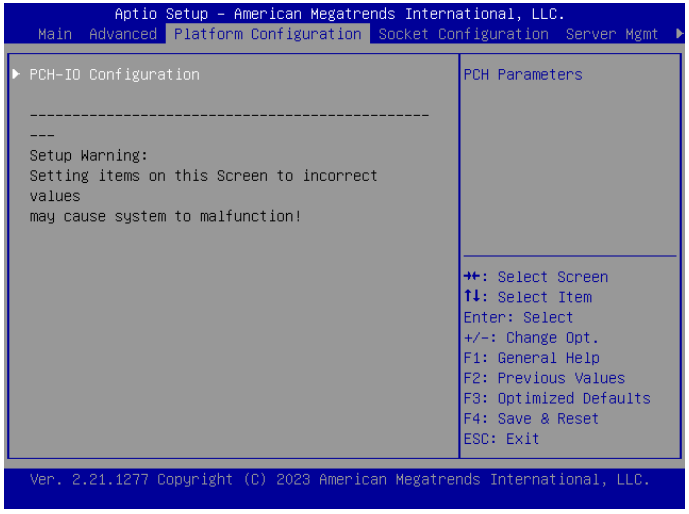


SDIO Access Mode

Auto option: Access SD device in DMA mode if controller supports it, otherwise in PIO mode.
DMA option: Access SD device in DMA mode.
PIO option: Access SD device in PIO mode.

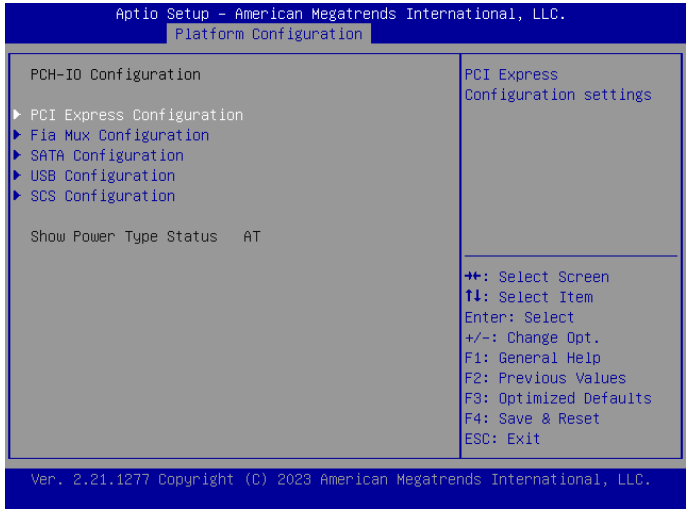
eMMC Device
Mass storage device emulation type. "Auto" enumerates devices less than 530MB as floppies. Forced FDD option can be used to force HDD formatted drive to boot as FDD.

Platform Configuration



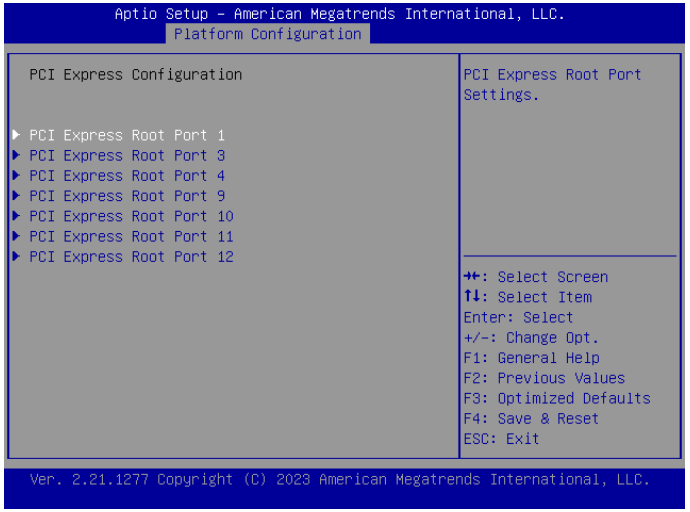
PCH Configuration
Enter the PCH Configuration submenu.

PCH-IO Configuration



PCI Express Configuration / Fia Mux Configuration / SATA Configuration / USB Configuration / SCS Configuration
Press **Enter** to access each submenu.

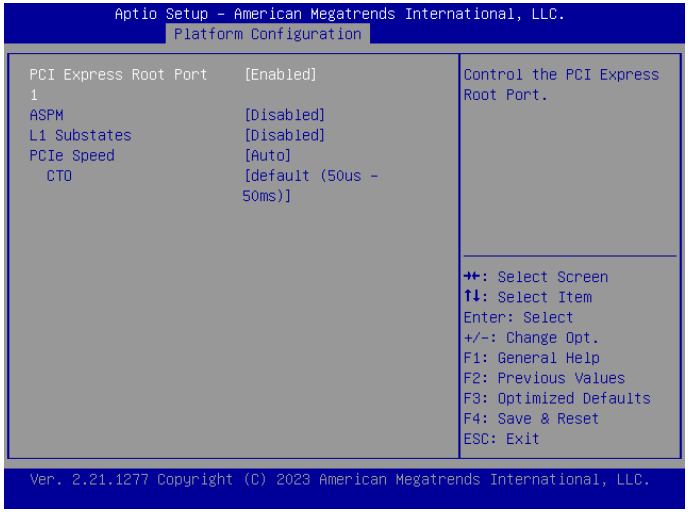
PCI Express Configuration



PCI Express Root Port 1~12

Press **Enter** to access each submenu and configure each option.

PCI Express Configuration > PCI Express Root Port



PCI Express Root Port
Enable or disable the PCI Express port.

ASPM Support
Select the ASPM level.

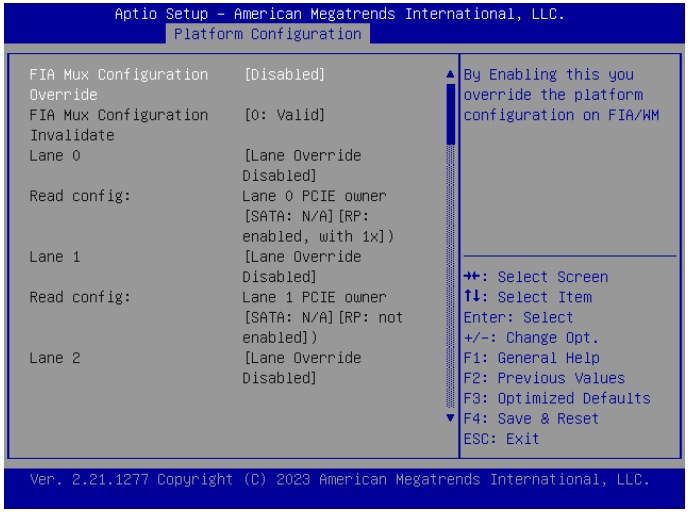
Force L0	Forces all links to L0 state.
Auto	The BIOS automatically selects an ASPM level.
Disable	Disables ASPM

L1 Substates
Configure the L1 Substates settings.

PCIe Speed
Configure the speed of the PCI Express port.

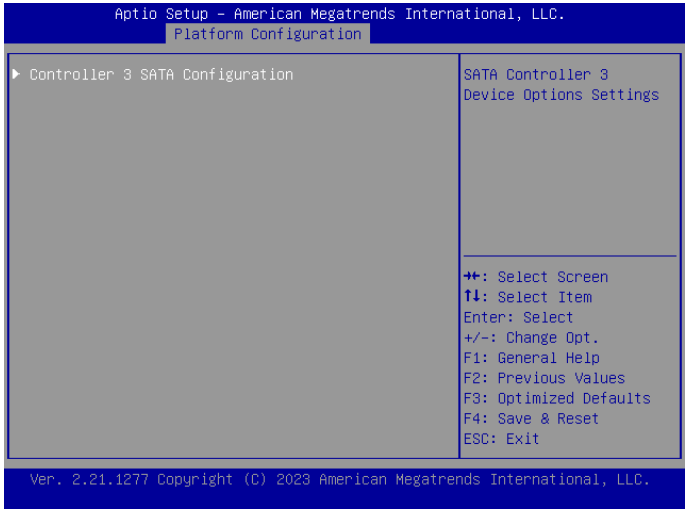
CT0
Configure the CT0 for PCI Express.

FIA Mux Configuration



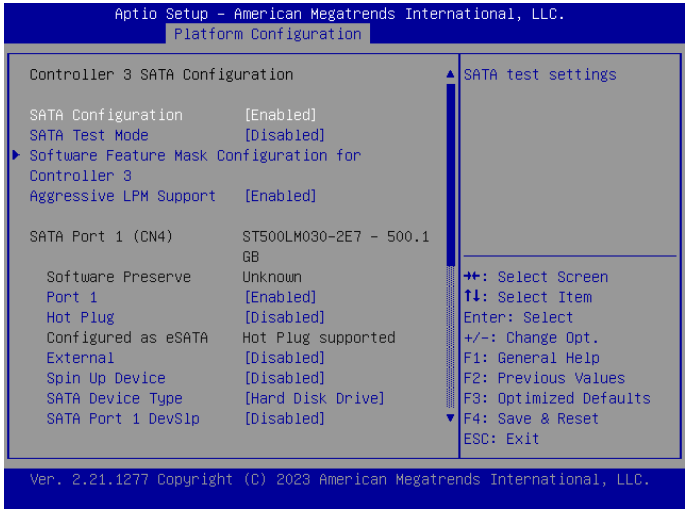
FIA Mux Configuration
By enabling this you override the platform configuration on FIA/WM.

SATA Configuration



Controller 3 SATA Configuration
Enter the Controller 3 SATA Configuration submenu.

SATA Configuration > Controller 3 SATA Configuration



SATA Configuration
Enable or disable SATA configuration.

SATA Test Mode
Enable or disable SATA test mode.

Software Feature Mask Configuration for Controller 3
Enable or disable software feature mask configuration for controller 3.

Aggressive LPM Support
Enable or disable aggressive LPM support.

Port 1/3
Enable or disable SATA port 1/3.

Hot Plug
Enable or disable hot plugging feature on SATA port 1/3.

External
Enable or disable the feature of External.

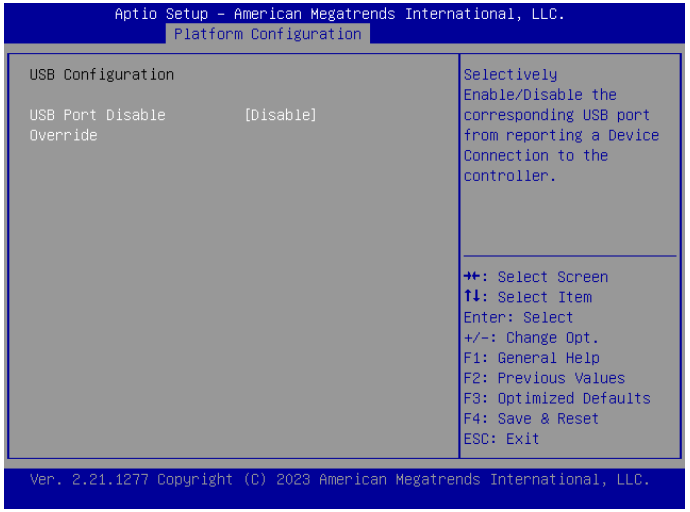
Spin Up Device
Enable or disable staggered spin up on devices connected to SATA port 1/3.

SATA Device Type
Identiy what type of SATA device is connected.

SATA Port 1/3 DevSlp
Enable or disable SATA Port 1/3 DevSlp. Before enabling DevSlp, board rework is needed.

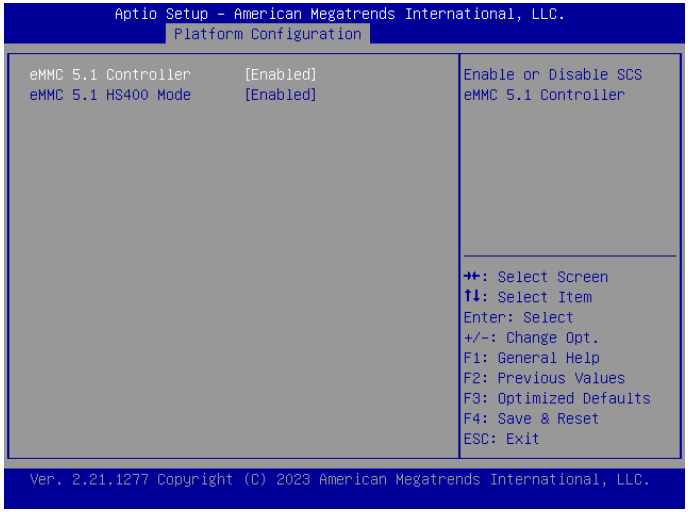
DITO Configuration
Enable or disable DITO configuration.

USB Configuration



USB Port Disable Override
Selectively enable or disable the corresponding USB port from reporting a device connection to the controller.

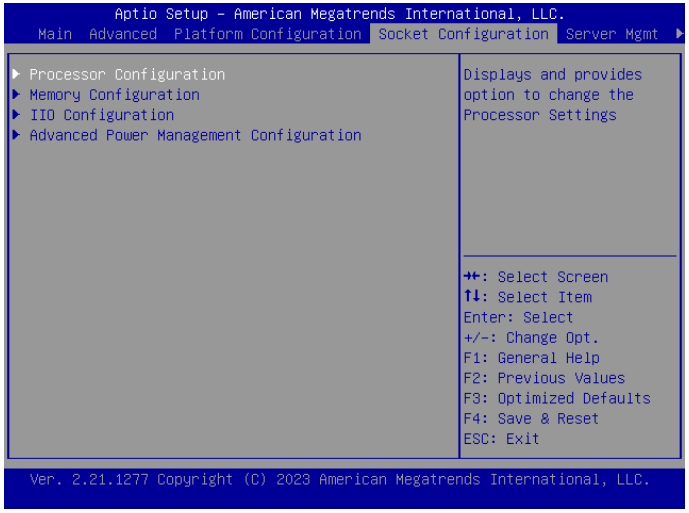
SCS Configuration



eMMC 5.1 Controller
Enable or disable SCS eMMC 5.1 controller.

eMMC 5.1 HS400 Mode
Enable or disable eMMC 5.1 HS400 mode.

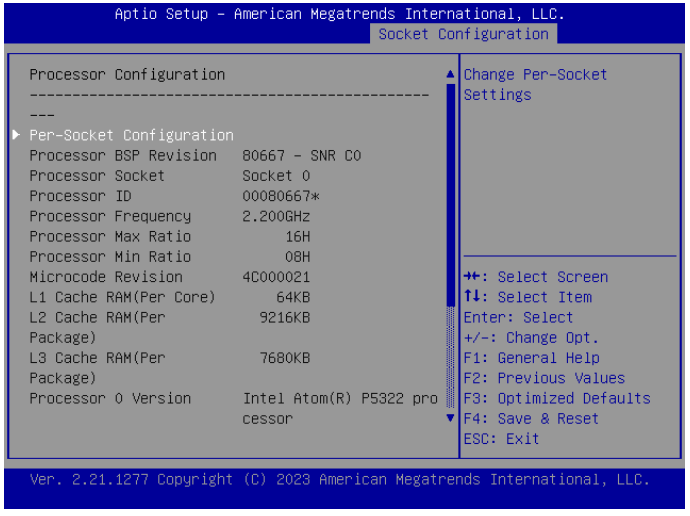
Socket Configuration



Processor Configuration / Memory Configuration / IIO Configuration / Advanced Power Management Configuration

Press **Enter** to access each submenu.

Processor Configuration



Pre-Socker Configuration
Change pre-socket settings.

Max CPUID Value Limit
Set this field to Disable when using Windows XP. Set this field to Enable when using legacy operating systems so that the system will boot even when it doesn't support CPUs with extended CPUID function.

Hardware Prefetcher
Enable or disable the MLC streamer prefetcher.

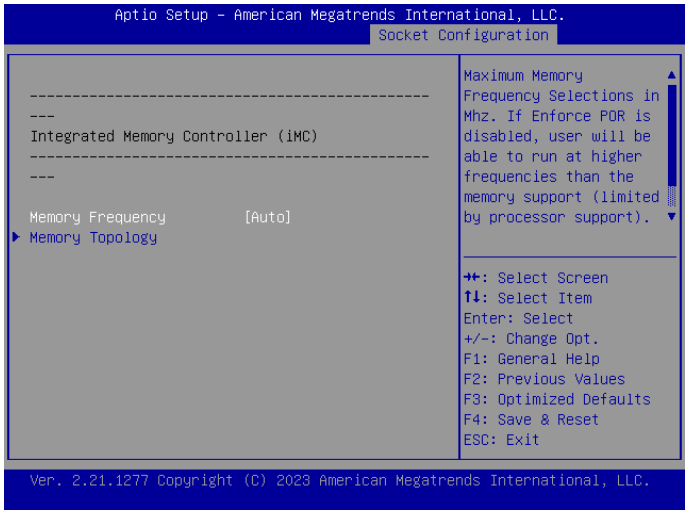
Adjacent Cache Prefetch
Enable or disable the adjacent cache prefetch.

Extended APIC
Enable or disable extended APIC support.

VMX
When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Enable SMX
Enable or disable Secure Mode Extensions.

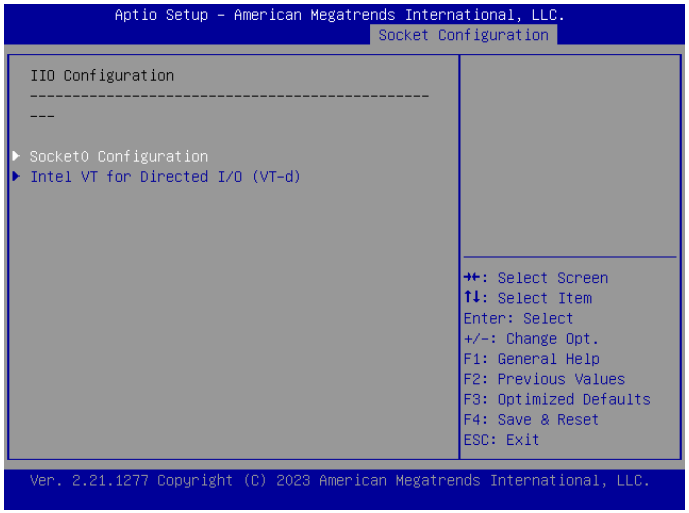
Memory Configuration



Memory Frequency
Configure the maximum frequency of the memory. Do not select Reserved.

Memory Topology
Press **Enter** to see the information on the memory installed.

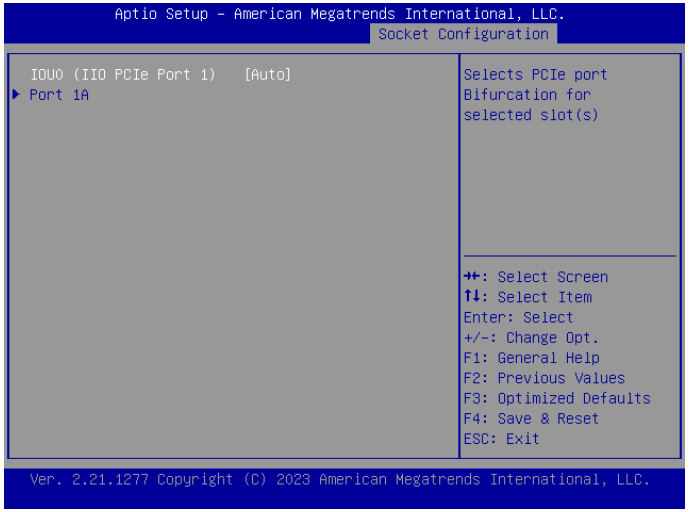
IIO Configuration



Socket0 Configuration
Enter the Socket0 Configuration submenu.

Intel VT for Directed I/O (VT-d)
Enter the Intel VT for Directed I/O (VT-d) submenu.

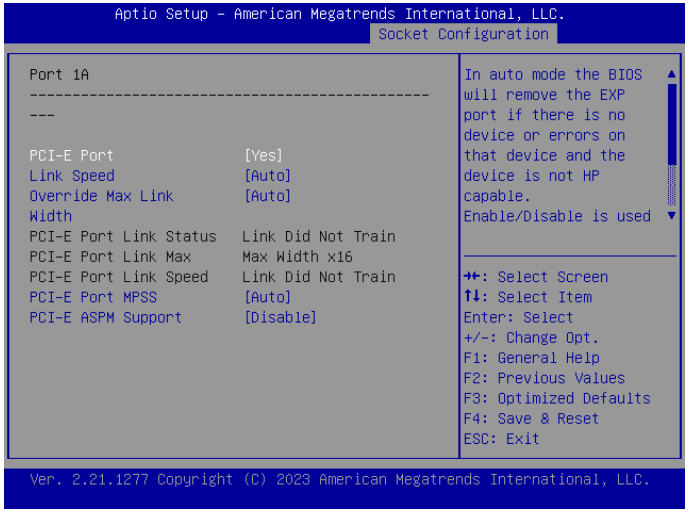
Socket0 Configuration



IOU0 (II0 PCIe Port 1)
Select PCIe port bifurcation for selected slot(s).

Port 1A
Enter the Port 1A submenu.

Socket0 Configuration > Port 1 A



PCI-E Port
Enable or disable the PCIe port. In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space

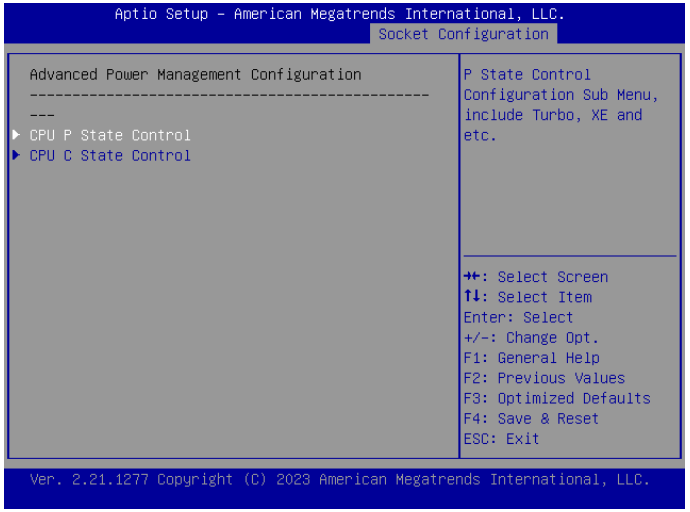
Link Speed
Configure the link speed for the PCIe port.

Override Max Link Width
Configure the link speed to override the max link width set by bifurcation.

PCI-E Port MPSS
Configure the PCI-e Port MPSS.

PCI-E ASPM Support
This option enables or disables the ASPM support for all downstream devices.

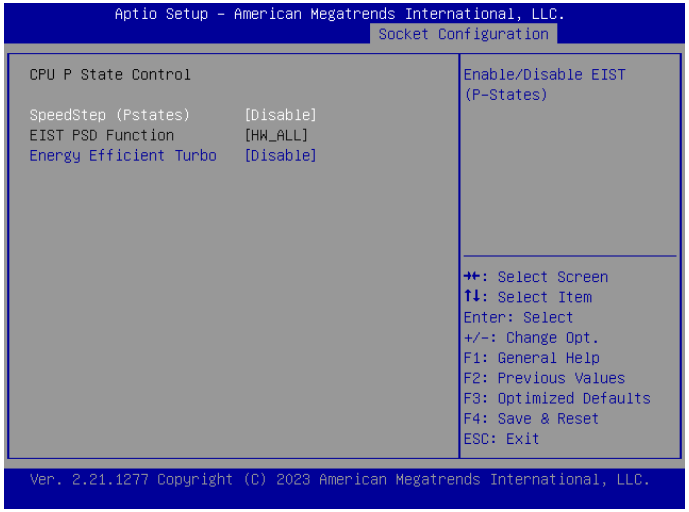
Advanced Power Management Configuration



CPU P State Control
Enter the CPU P State Control submenu.

CPU C State Control
Enter the CPU C State Control submenu.

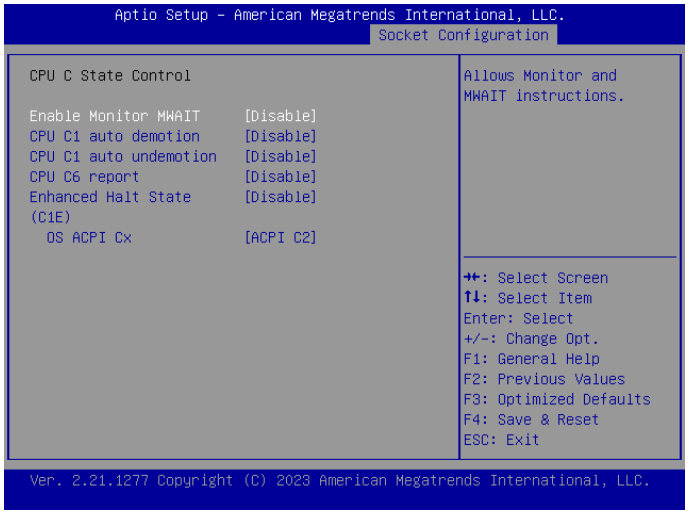
CPU P State Control



SpeedStep (Pstates)
Enable or disable EIST (P-States).

Energy Efficient Turbo
Enable or disable Energy Efficient Turbo.

CPU C State Control



Enable Monitor MWAIT
Enable or disable monitoring and MWAIT instructions.

CPU C1 auto demotion
Enable or disable CPU C1 auto demotion.

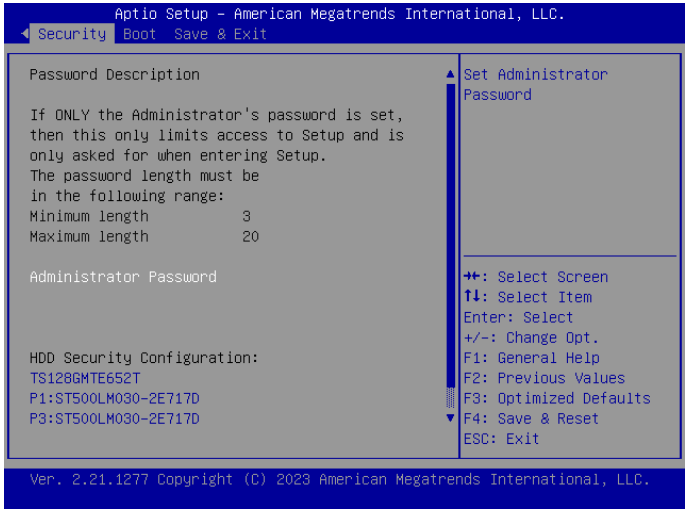
CPU C1 auto undemotion
Enable or disable CPU C1 auto undemotion.

CPU C6 report
Enable or disable C6 report to the operating system.

Enhanced Halt State (C1E)
Enable or disable Enhanced Halt State (C1E) for lower power consumption.

OS ACPI Cx
Enable or disable C3 report or C6 report to OS ACPI C2 or ACPI C3.

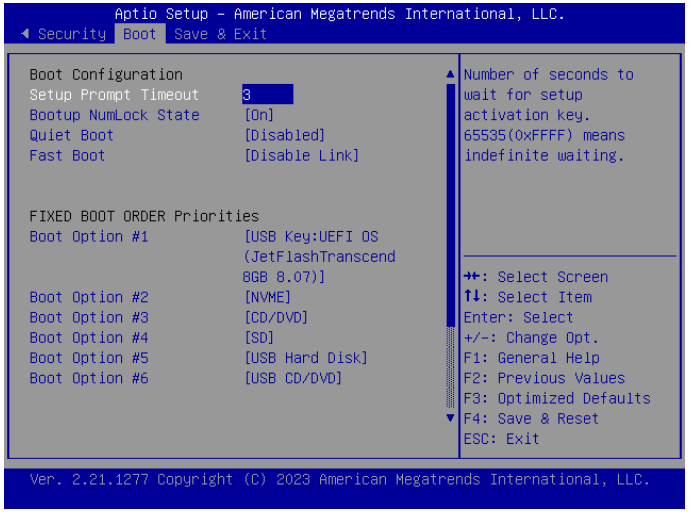
Security



Administrator Password

Set the administrator's password for the system.

Boot



Setup Prompt Timeout
Select the number of seconds to wait for the setup activation key. 65535(0xFFFF) denotes indefinite waiting.

Bootup NumLock State
This allows you to determine the default state of the numeric keypad. By default, the system boots up with NumLock on wherein the function of the numeric keypad is the number keys. When set to Off, the function of the numeric keypad is the arrow keys.

Quiet Boot
Enable or disable the quiet boot function.

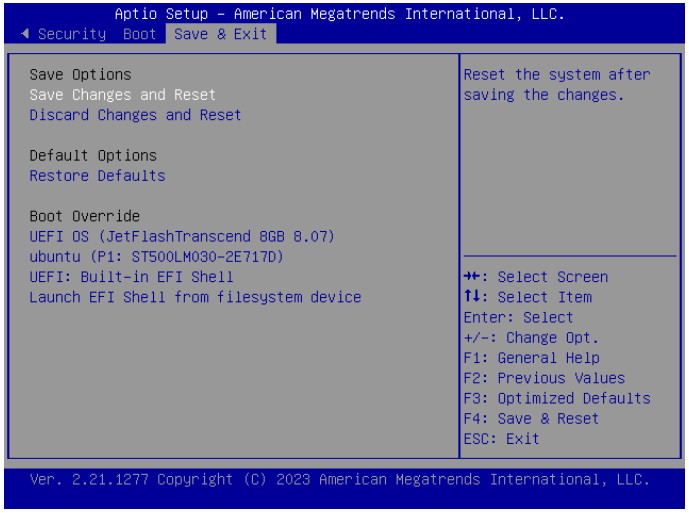
Fast Boot
Enable or disable boot with initialization of a minimal set of devices required to launch active boot option. This doesn't affect the BBS boot options.

Boot Option #1 ~ #X
Select the boot sequence of the hard drives. X represents the quantity of connected devices.

UEFI Hard Disk Drive BBS Priorities
Configure the boot device priority sequence from available UEFI hard disk drives.

UEFI USB Key Drive BBS Priorities
Configure the boot device priority sequence from available UEFI USB key drives.

Save & Exit



Save Changes and Reset
To save the changes and reset, select this field then press <Enter>. A dialog box will appear. Confirm by selecting Yes.

Discard Changes and Exit
To exit the Setup utility without saving the changes, select this field then press <Enter>. You may be prompted to confirm again before exiting. You can also press <ESC> to exit without saving the changes.

Restore Defaults
To restore the BIOS to default settings, select this field then press <Enter>. A dialog box will appear. Confirm by selecting Yes.

Boot Override
To bypass the boot sequence from the Boot Option List and boot from a particular device, select the desired device and press <Enter>.